Industrial Grade
-X00S series
CFast Card

Preliminary Product
Manual

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www.cactus-tech.com

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1.Introduction to Cactus Technologies® Industrial Grade -X00S Series CFast Products

Features:

- Solid state design with no moving parts

- Industry standard CFast Type I form factor

- Capacities from 1GB to 64GB

- Compliant with Serial ATA 3.3 specifications

- ATA-8 compatible and CFast 2.0 compliant

- Supports Serial ATA Generation I/II/III interface rate of 1.5/3.0/6.0Gbps

- Support ATA SMART Feature Set

- Support ATA Security Feature Set

- End to End Datapath protection

- SRAM ECC for SEU protection

- ECC capable of correcting up to 96 random bit errors per 1KB or 120 random bit errors per 2KB

- Enhanced error correction, < 1 error in 10^{14} bits read

- SATA partial and slumber modes and DEVSLP mode supported

- Voltage support: 3.3V±5%

Cactus Technologies® CFast card is a high capacity solid-state flash memory product that complies with the Serial ATA 3.3 standard and is functionally compatible with a SATA hard disk drive. Cactus Technologies® CFast cards provide up to 64GB of formatted storage capacity.

Cactus Technologies® CFast product uses high quality SLC NAND flash memory from Kioxia Corporation. In addition, it includes an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller's firmware is upgradeable, thus allowing feature enhancements and firmware updates while keeping the BOM stable.

1.1.   Supported Standards

Cactus Technologies® Industrial CFast card is fully compatible with the following specification:

- ATA 8 Specification published by ANSI
- Serial ATA 3.3 Specification published by the Serial ATA International Organization
- CFast 2.0 Specification published by CFA

1.2.   Product Features

Cactus Technologies® Industrial CFast card contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1.   Host and Technology Independence

Cactus Technologies® Industrial CFast card appears as a standard SATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the SATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies® Industrial CFast products today will continue to work with future Cactus Technologies® Industrial CFast cards built with new flash technology without having to update or change host software.

1.2.2.   Defect and Error Management

Cactus Technologies® Industrial CFast card contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Industrial CFast card is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Industrial CFast cards unparalleled reliability.

1.2.3. Power Supply Requirements

Cactus Technologies® Industrial CFast card operates at a voltage range of 3.3 volts ± 5%.

2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® Industrial CFast
Temperature	Operating:	0° C to +70° C (Standard) -40° C to +85° C (Extended)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Vibration	Non-Operating:	16.4G, MIL-STD-810F Method 514.5, Procedure 1
Shock	Operating & Non-Operating:	50 G, MIL-STD-810F Method 516.5, Procedure 1
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® Industrial CFast
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		3.3V ±5%
(Maximum Average Value) See Notes.	Sleep: Reading: Writing:	35 mA 395 mA 320 mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a "Not Busy" operating state.

2.3. System Performance

All performance timings assume the drive controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

	1G	2G	4G	8G	16G	32G	64G
Read Transfer Rate (sequential)	30MB/s	60MB/s	65MB/s	255MB/s	255MB/s	270MB/s	320MB/s
Write Transfer Rate (sequential)	20MB/s	30MB/s	45MB/s	60MB/s	100MB/s	125MB/s	135MB/s

.

2.4. System Reliability

Table 2-4. Reliability

Data Reliability	< 1 non-recoverable error in 10^{14} bits READ	
Endurance (Estimated TBW):	**Large Block Sequential workload**	**JEDEC 219 Enterprise workload**
1G	60TB	12TB
2G	120TB	23TB
4G	240TB	46TB
8G	480TB	92TB
16G	960TB	184TB
32G	1920TB	368TB
64G	3840TB	737TB

Note: Estimation is based on testing at room temperature only and without consideration of data retention.

2.5. Physical Specifications

The following sections provide the physical specifications for Cactus Technologies® Industrial CFast products.

2.5.1. CFast Card Physical Specifications

Table 1: Type I CFast Card Physical Specifications

Length:	36.4 ± 0.15 mm (1.433 ±.006 in.)
Width:	42.80 ± 0.10 mm (1.685 ±.004 in.)
Thickness Including Label Area:	3.6 mm maximum (.1418 in maximum).
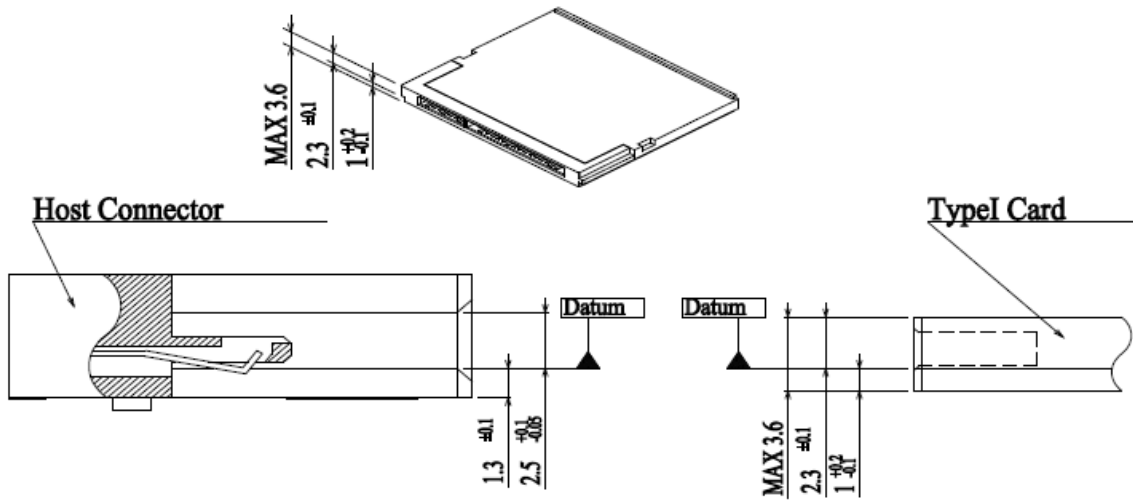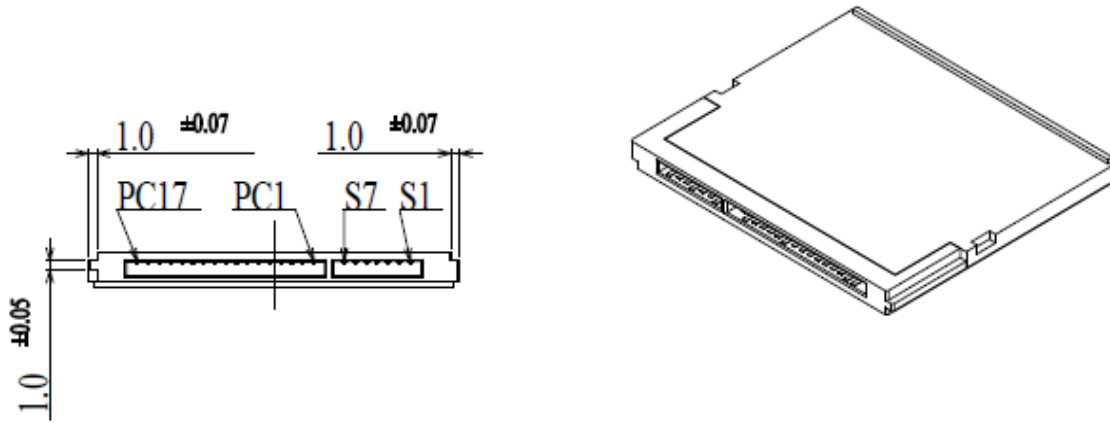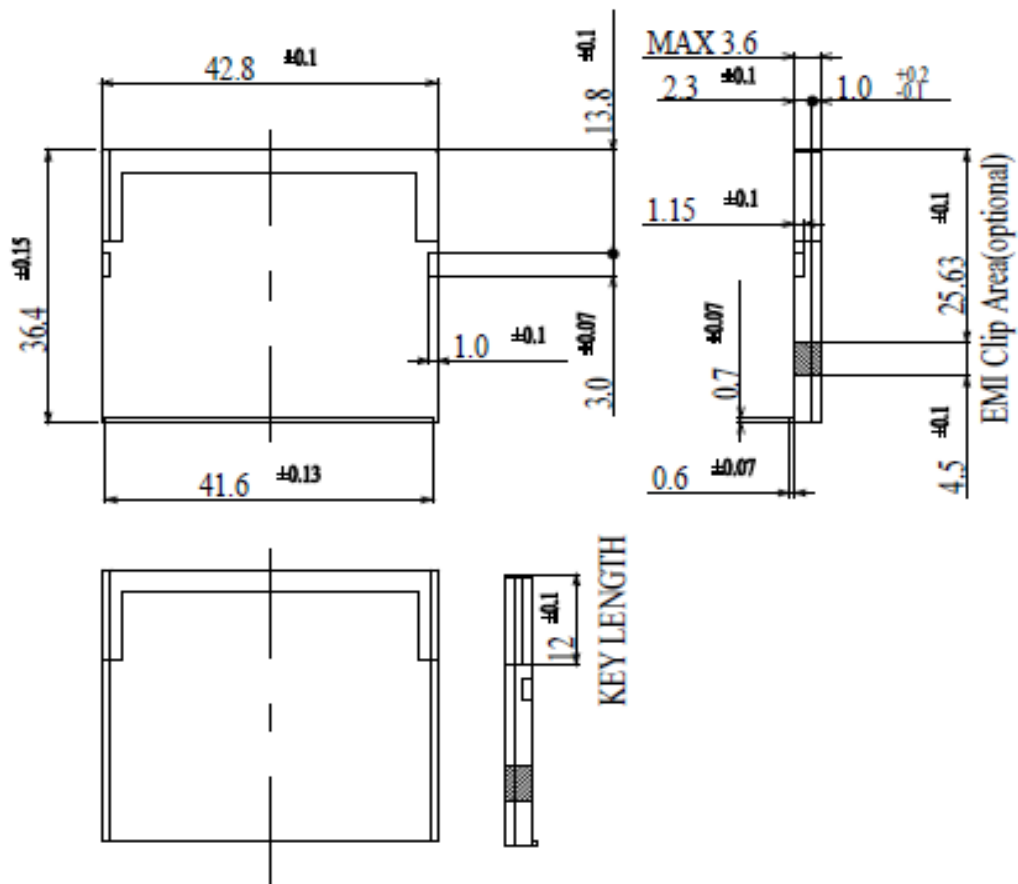
Figure 2-1. Type I CFast Card Dimensions

3. Interface Description

The following sections provide detailed information on the Cactus Technologies® Industrial CFast card interface.

3.1. CFast Pin Assignments and Pin Type

Cactus Technologies® CFast signal pinout conforms to CFA specifications. The signal/pin assignments and descriptions are listed in Table 3-5.

Table 3-5. CFast Pin Assignments and Pin Type

Number	Segment	Name	Type	Description	Mating Sequence
S1	SATA	SGND	Signal GND	Ground for signal integrity	1st
S2	SATA	A+	SATA Differential	Signal Pair A	2nd
S3	SATA	A-	SATA Differential		2nd
S4	SATA	SGND	Signal GND	Ground for signal integrity	1st
S5	SATA	B-	SATA Differential	Signal Pair B	2nd
S6	SATA	B+	SATA Differential		2nd
S7	SATA	SGND	Signal GND	Ground for signal integrity	1st
	Key				
	Key				
PC1	PWR/CTL	CDI	Input	Card Detect In	3rd
PC2	PWR/CTL	PGND	Device GND		1st
PC3	PWR/CTL	DEVSLP	DEVSLP Card Input	DevSleep Power State Enable	2nd
PC4	PWR/CTL			Reserved[1]	2nd
PC5	PWR/CTL			Reserved[1]	2nd
PC6	PWR/CTL			Reserved[1]	2nd
PC7	PWR/CTL	PGND	Device GND		1st
PC8	PWR/CTL	LED1	LED Output	LED Output [1]	2nd
PC9	PWR/CTL	LED2	LED Output	LED Output [1]	2nd
PC10	PWR/CTL			Reserved [1]	2nd
PC11	PWR/CTL			Reserved	2nd
PC12	PWR/CTL	IFDet	GND	Card output, connect to PGND on card[2]	2nd
PC13	PWR/CTL	PWR	3.3V	Device Power (3.3V)	2nd
PC14	PWR/CTL	PWR	3.3V	Device Power (3.3V)	2nd
PC15	PWR/CTL	PGND	Device GND	Device Ground	1st
PC16	PWR/CTL	PGND	Device GND	Device Ground	1st
PC17	PWR/CTL	CDO	Output	Card Detect Out	3rd [3]

Notes:
[1] The functionality of these pins is deprecated, and is included to provide backwards compatibility with CFast V1.1. The CFA plans to use these pins differently in the future. These pins should not be used by devices that are compliant with the CFast specification V2.0.
[2] IFDet shall be connected to PGND on all CFast V2.0 compliant devices.
[3] The connection of any pin is not reliable until CDO signals that the card is fully inserted.

3.2.   Electrical Specifications

The following table defines all D.C. Characteristics for the CFast products. Unless otherwise stated, conditions are:

Vcc = 3.3V ± 5%
Ta = -40°C to 85°C

3.2.1.   Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-55	+100	°C
Operating Temperature	T_A	-40	+85	°C
Vcc with respect to GND	Vcc	-0.3	3.6	V

3.2.2.   DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Operating Current	I_{CC}			mA
Idle			40	
Active			400	

3.2.3.   AC Characteristics

Cactus Technologies® CFast products conforms to all AC timing requirements as specified in the CFA specifications. Please refer to that document for details of AC timing for all operation modes of the device.

4. ATA Drive Register Set Definition and Protocol

The communication to or from the CFast card is done using FIS. Legacy ATA protocol is supported by using the legacy mode defined in the SATA specifications. In this mode, the FIS has defined fields which provide all the necessary ATA task file registers for control and status information. The Serial ATA interface does not support Primary/Secondary or Master/Slave configurations. Each SATA channel supports only one SATA device, with the register selection as defined by the ATA standard.

4.1. ATA Task File Definitions

The following sections describes the usage of the ATA task file registers. Note that the Alternate Status Register of legacy ATA is not defined for SATA drives.

4.1.1. Data Register

The Data Register is a 16-bit register, and it is used to transfer data blocks between the SSD data buffer and the Host.

4.1.2. Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK)   This bit is set when a Bad Block is detected.

Bit 6 (UNC)   This bit is set when an Uncorrectable Error is encountered.

Bit 5   This bit is 0.

Bit 4 (IDNF)   The requested sector ID is in error or cannot be found.

Bit 3   This bit is 0.

Bit 2 (Abort)   This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1   This bit is 0.

Bit 0 (AMNF)   This bit is set in case of a general error.

4.1.3. Feature Register

This register provides information regarding features of the SSD that the host can utilize.

4.1.4. Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SSD. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.1.5. Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SSD data access for the subsequent command.

4.1.6. Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.1.7. Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.1.8. Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7   This bit is set to 1.
Bit 6   LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5   This bit is set to 1.
Bit 4 (DRV)   DRV is the drive number. This should always be set to 0.
Bit 3 (HS3)   When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2)   When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1)   When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0)   When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.1.9.   Status Registers

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY)   The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY)   RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.

Bit 5 (DWF)   This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC)   This bit is set when the device is ready.

Bit 3 (DRQ)   The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR)   This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX)   This bit is always set to 0.

Bit 0 (ERR)   This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.1.10.   Device Control Register

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HOB	X	X	X	1	SW Rst	-IEn	0

Bit 7   This bit is used in 48-bit addressing mode. When cleared, the host can read the most recently written values of the Sector Count,Drive/Head and LBA registers. When set, the host will read the previous written values of these registers. A write to any Command block register will clear this bit.

Bit 6   This bit is an X (Do not care).

Bit 5   This bit is an X (Do not care).

Bit 4   This bit is an X (Do not care).

Bit 3   This bit is ignored by the drive.

Bit 2 (SW Rst)   This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn)   The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0   This bit is ignored by the drive.

4.1.11.   Drive Address Register

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7   This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SSD. Following are some possible solutions to this problem:
1. Locate the SSD at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a SSD in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SSD product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SSD's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SSD or b) if provided use an additional Primary/Secondary configuration in the SSD that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG)   This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3)   This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2)   This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1)   This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0)   This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1)   This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0)   This bit is 0 when the drive 0 is active and selected.

5. ATA Command Description

This section defines the ATA command set supported by Cactus Technologies® CFast card.

5.1.   ATA Command Set

Table 5-6 summarizes the supported ATA command set .

Table 5-6. ATA Command Set

COMMAND	Code
Check Power Mode	E5h, 98h
Data Set Management	06h
Download Microcode	92h
Download Microcode DMA	93h
Erase All Blocks	C3h
Erase Sector(s)	C0h
Execute Drive Diagnostic	90h
Flush Cache	E7h
Flush Cache Ext	EAh
Format Track	50h
Identify Drive	ECh
Idle	E3h, 97h
Idle Immediate	E1h, 95h
Initialize Drive Parameters	91h
Media Lock	DEh
Media Unlock	DFh
NOP	00h
Read Buffer	E4h
Read DMA	C8h, C9h
Read DMA Ext	25h
Read FPDMA Ext	60h
Read Log Ext	2Fh
Read Log DMA Ext	47h
Read Multiple	C4h
Read Multiple Ext	29h
Read Native Max Address	F8h
Read Native Max Address Ext	27h
Read Sector(s)	20h, 21h
Read Sector(s) Ext	24h
Read Verify Sector(s)	40h, 41h
Read Verify Sector(s) Ext	42h
Recalibrate	1Xh
Request Sense	03h
Security Disable Password	F6h
Security Erase Prepare	F3h
Security Erase Unit	F4h
Security Freeze Lock	F5h
Security Set Password	F1h
Security Unlock	F2h
Seek	7Xh
Set Features	EFh
Set Max Address	F9h
Set Max Address Ext	37h
Set Multiple Mode	C6h
Set Sleep Mode	E6h, 99h
SMART	B0h
Stand By	E2h, 96h
Stand By Immediate	E0h, 94h
Translate Sector	87h
Write Buffer	E8h
Write DMA	CAh, CBh
Write DMA Ext	35h
Write FPDMA Ext	61h

COMMAND	Code
Write DMA FUA Ext	3Dh
Write Log Ext	3Fh
Write Log DMA Ext	57h
Write Multiple	C5h
Write Multiple Ext	39h
Write Multiple FUA Ext	CEh
Write Multiple w/o Erase	CDh
Write Sector(s)	30h, 31h
Write Sector(s) Ext	34h
Write Sector(s) w/o Erase	38h
Write Verify	3Ch

5.1.1. Erase All Blocks - C3h

The Erase All Blocks command can be used to erase all User blocks or all Physical blocks of the card. If the value in Sector Number register is set to 0, all user and buffer blocks are erased. If the value is set to 1, all physical blocks except for the manufacturer defect blocks are erased.

If the Erase All Block command execution is interrupted by power loss, the erase operation will resume upon power on.

5.1.2. Set Features - EFh

The following features are supported by Cactus Technologies® CFast card:

Feature Code	Description
02h, 82h	Enable/Disable write cache (Note: this feature has no effect as Cactus Technologies® CFast card does not use write caching.)
03h	Set transfer mode
05h, 85h	Enable/Disable advanced power management
09h, 89h	Enable/Disable Active Power Management
0Ah, 8Ah	Enable/Disable power level 1 commands
55h, AAh	Disable/Enable Read Look Ahead
66h, CCh	Disable/Enable Power On Reset establishment of defaults at Soft Reset
69h	NOP – accepted for backwards compatibility
96h	NOP – accepted for backwards compatibility
97h	Accepted for backwards compatibility

Feature Code	Description
9Ah	Set the host current source capability
BBh	4 bytes of data apply on Read/Write Long commands
10h, 90h	Enable/Disable SATA feature selected by the Count Register. The supported features are: 01h – Non-zero Buffer Offsets 02h – DMA Setup FIS Auto-Activate optimization 03h – DMA Setup FIS Auto-Activate optimization 04h – Guarantted In-Order Data Delivery 06h – Software Settings Preservation 07h – Device Automatic Partial to Slumber transition 09h – Device Sleep 0Bh – Power Disable Feature

5.1.3.   Identify Drive—ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-7. All reserved bits or words are zero. Table 5-7 is the definition for each field in the Identify Drive Information.

Table 5-7. Identify Drive Information

Word Address	Default Value	Total Bytes	Data Field Type Information
0	045AH	2	General configuration bit-significant information.
1	XXXXH	2	Default number of cylinders; capacity dependent.
2	C837H	2	Specific configuration.
3	00XXH	2	Default number of heads; capacity dependent.
4-5	0000H	4	Reserved
6	XXXXH	2	Default number of sectors per track; capacity dependent.
7-8	XXXXH	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW); capacity dependent.
9	0000H	2	Reserved.
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20-21	0000H	4	Reserved.
22	0000H	2	# of ECC bytes passed in R/W Long commands
23-26	aaaa	8	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	8001H	2	Maximum number of sectors on Read/Write Multiple command: 1
48	4000H	2	Trusted Computing feature set options.
49	0F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4001H	2	Capabilities: device specific standby timer minimum
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0007H	2	Data fields 54-58,64-70 and 88 are valid.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.

Word Address	Default Value	Total Bytes	Data Field Type Information
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	010XH	2	Multiple sector setting is valid; low byte is capacity dependent.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000H	2	Single Word DMA transfer not implemented
63	0X0XH	2	Multiword DMA modes 0-2 are supported; upper byte reflects currently selected MWDMA mode.
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum MWDMA cycle time per word is 120ns.
66	0078H	2	Recommended MWDMA cycle time is 120ns.
67	0078H	2	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	2	Minimum PIO cycle time with IORDY flow control is 120ns.
69	4100H	2	Deterministic read after DSM Trim, Download Microcode DMA supported.
70-74	0000H	10	Reserved
75	001FH	2	Queue depth of 32 for NCQ
76	C10EH	2	SATA Capabilities: Read LOG DMA Ext, Device Automatic Partial to Slumber transition, NCQ, Gen 1, Gen2, Gen3 signaling rates
77	00CXH	2	SATA Additional Capabilities: DevSleep, RECEIVE FPDMA QUEUED, SEND FPDMA QUEUED
78	015EH	2	SATA features supported: Device Sleep, Software settings preservation, in-order data delivery, device initiated interface power management, DMA Setup Auto-Activate, non-zero buffer offsets supported.
79	0XXXH	2	SATA features enabled.
80	0FE0H	2	Supports ATA5 to ATA8, ACS-1 to ACS-4
81	0000H	2	No minor revision reported.
82	746BH	2	Command set: NOP, READ BUFFER, WRITE BUFFER, HPA, look-ahead, volatile write cache, power management feature set, Security Mode feature set, SMART feature set
83	7509H	2	Command Set: Flush Cache/Flush Cache Ext, LAB48, Set Max Security Extension, Advanced Power Management, microcode download
84	4161H	2	Command Set: World wide name, Write FUA Ext, general purpose logging, SMART self-test, SMART error logging
85	74XXH	2	Command Set enabled.
86	F409H	2	Command Set enabled.
87	4161H	2	Command Set edfault.
88	XXXXH	2	UDMA Modes enabled and supported.
89	00XXH	2	Time for Security Erase Unit not specified.
90	00XXH	2	Time for Enhanced Security Erase Unit not specified.
91	00XXH	2	Advanced Power Management Level
92	XXXXH	2	Master password revision code
93	XXXXH	2	Hardware Reset Result
94-99	0000H	12	Reserved
100-103	XXXXH	8	Maximum user LBA for 48-bit addressing mode.
104	0000H	2	Reserved
105	0001H	2	# of sectors per Data Set Management command.
106	4000H	2	Physical Sector Size/Logical sector size
107	0000H	2	Reserved
108-111	XXXXH	8	Word Wide Name
112-118	0000H	14	Reserved
119	4008H	2	Command/Feature set supported extension.
120	4008H	2	Command/Feature set enabled extension.
121-127	0000H	14	Reserved
128	0XXXH	2	Security status
129	XX00H	2	Write Protect status: Bit 9: Permanent write protect due to vendor command Bit 8: Temporary write protect due to vendor command
130-133	aaaa	8	Firmware date string
134-135	0000H	4	Reserved
136-141	aaaa	12	Firmware file name
142-147	aaaa	12	Preformat file name

Word Address	Default Value	Total Bytes	Data Field Type Information
148-153	aaaa	12	Anchor program file name
154	0000H	2	Firmware major revision
155	0000H	2	Firmware minor revision
156-168	0000H	78	Reserved
169	0001H	2	TRIM bit in Data Set Management supported
170-208	0000H	78	Reserved
209	4000H	2	Alignment of logical blocks within a larger physical block
210-216	0000H	14	Reserved
217	0001H	2	Solid State Device
218-221	0000H	8	Reserved
222	11FFH	2	Transport major version: ATA8-AST, SATA 1.0-3.3
223	0000H	2	Transport minor version not supported
224-254	0000H	62	Reserved
255	XXA5H	2	Integrity word

6. S.M.A.R.T. Support

Cactus Technologies® -X00S Series CFast cards support S.M.A.R.T. Status and attribute reporting functions as determined by the value of the Feature Register. The S.M.A.R.T. subcommands supported are as follows:

Code	Sub Command
D0	Read Data
D1	Read Attribute Thresholds
D2	Enable/Disable Attribute Autodave
D5	Read Log
D6	Write Log
D8	Enable Operations
D9	Disable Operations
DA	Return Status
E0	Read Remap Data

The general format for issuing a SMART command is as follows:

Register	7	6	5	4	3	2	1	0
Feature	Subcommand code							
Sector Count								
Sector Number								
Cyliner Low	4Fh							
Cylinder High	C2h							

Register	7	6	5	4	3	2	1	0
Drive/Head	1	1	1	D				
Command	B0h							

6.1. S.M.A.R.T. Enable Operations

Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters.

6.2. S.M.A.R.T. Disable Operations

Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on. Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

6.3. S.M.A.R.T. Enable/Disable Attribute Autosave

This subcommand is issued with the Sector Count register set to either 00h or F1h. 00h enables Autosave while F1h disables it. However, this is in affect a NOP as the SMART attributes are always auto-saved.

6.4. S.M.A.R.T. Read Data

This subcommand returns 512 bytes of S.M.A.R.T. data structure. When this subcommand is issued, the Feature Register must contain D0h, the LBA Mid register must contain 4Fh and the LBA high register must contain C2h. The returned data has the following structure:

Byte	Value	Description
0-1	0010h	SMART structure revision number
2-361		1st – 30th attribute data (12 bytes each)
362	00h	Offline data collection status (no offline data collection)
363		Selftest execution status
364-365	0000h	Total time in seconds to complete offline data collection

Byte	Value	Description
366	00h	Reserved
367	00h	Offline data collection capability (no offline data collection)
368-369	0003h	S.M.A.R.T. Capability
370	00h	Error logging capability (no error logging capability)
371	00h	Reserved
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374-385	00h	Reserved
386-387	0004h	SMART structure version
388-391		Firmware "Commit" counter
392-395		Firmware Wear Level Threshold
396		"1" : Global Wear Leveling active
397		"1" : Global Bad Block Management active
398-401		Reserved
402-405		Number of Flash Blocks involved in Wear Leveling in all block pools
406-409		Number of total ECC errors in all block pools during firmware initialization
410-413		Number of correctable ECC errors in all block pools during firmware initialization
414-510	00h	Reserved
511		checksum

6.5.   S.M.A.R.T. Attributes

The -X00S series CFast card monitors the attributes as shown in the following table:

ID	Description
196	Spare block count
213	Spare block count worse channel
229	Erase count
203	ECC error count
204	Corrected ECC error count

ID	Description
214	Anchor Block Status
216	Main Memory ECC error count
217	Main Memory ECC error count in Firmware Memory
199	UDMA CRC error count
232	Number of reads
12	Power on count
241	Total LBAs written
242	Total LBAs read
215	Trim Status
194	Temperature Status
184	E2E Data Path Protection ECC Count from Flash to SATA Interface
185	E2E Data Path Protection ECC Count from SATA Interface to Flash

The following tables lists the returned data for each reported attribute.

Attribute 196: Spare Block Count		
Byte	Value	Description
0	196	Attribute ID
1-2	0013h	Flags – Pre-fail type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value – percentage of remaing spare blocks summed over all the flash chips (100 x current spare blocks / initial spare blocks)
4		Attribute value (worst value)
5-7		Sum of the initial spare blocks over all flash chips
8-10		Sum of the current spare blocks over all flash chips
11	00h	Reserved

Attribute 213: Spare Block Count Worst Channel		
Byte	Value	Description
0	213	Attribute ID
1-2	0013h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value – percentage of remaining spare blocks from the worst flash channels (100 x current spare blocks / initial spare blocks)

Byte	Value	Description
4	64h	Attribute value (worse value).
5-7		Initial number of spare blocks of the flash channel with the worse current spare block count.
8-10		Current number of spare blocks of the flash channel with the worse current spare block count.
11	00h	Reserved

Attribute 229: Erase Count		
Byte	**Value**	**Description**
0	229	Attribute ID
1-2	001Xh	Flags – Pre-fail or Advisory type, attribute value is updated during normal operation, attribute is an event count
3		Attribute value. The value is the estimate of the percentage of remaining life based on the number of block erases compared to the target erase cycles per flash block.
4		Attribute value (worse value)
5-10		Estimated total number of block erases
11		Reserved

Attribute 203 : Total ECC Error Count		
Byte	**Value**	**Description**
0	203	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of ECC errors (correctable and uncorrectable)
9-10		--
11	00h	Reserved

Attribute 204 : Correctable ECC Error Count		
Byte	Value	Description
0	204	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of correctable ECC errors.
9-10		--
11	00h	Reserved

Attribute 214 : Anchor Block Status		
Byte	Value	Description
0	214	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation.
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Anchor block write count.
9-10		--
11	00h	Reserved

Attribute 216 : Total Main Memory ECC Error Count		
Byte	Value	Description
0	216	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of main memory ECC errors.
9-10		--
11	00h	Reserved

Attribute 217 : Total Main Memory ECC Error Count in Firmware Memory		
Byte	Value	Description
0	217	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of main memory ECC errors that could be corrected that are located in firmware memory.
9-11	00h	Reserved

Attribute 199 : UDMA CRC Error Count		
Byte	Value	Description
0	199	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate.
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of SATA CRC errors.
9-10		--
11	00h	Reserved

Attribute 232 : Total number of reads		
Byte	Value	Description
0	232	Attribute ID
1-2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count.
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-10		Total number of flash read commands.
11	00h	Reserved

Attribute 12 : Power On Count		
Byte	**Value**	**Description**
0	12	Attribute ID
1-2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count.
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-8		Total number of power on cycles.
9-10		--
11	00h	Reserved

Attribute 241 : Total LBAs Written (in units of 32MB)		
Byte	**Value**	**Description**
0	241	Attribute ID
1-2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count.
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-10		Total number of LBAs written, divided by 65536.
11	00h	Reserved

Attribute 242 : Total LBAs Read (in units of 32MB)		
Byte	**Value**	**Description**
0	242	Attribute ID
1-2	0012h	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count.
3	64h	Attribute value; this is fixed at 100.
4	64h	Attribute value (worse value).
5-10		Total number of LBAs read, divided by 65536.
11	00h	Reserved

Attribute 215 : TRIM Status

Byte	Value	Description
0	215	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value.
4		Attribute value (worse value).
5-10		--
11	00h	Reserved

Attribute 194 : Temperature Status

Byte	Value	Description
0	194	Attribute ID
1-2	0002h	Flags – Advisory type, attribute value is updated during normal operation
3		Attribute value.
4		Attribute value (worse value).
5		Current temperature.
6		Min. temperature.
7		Max. temperature.
8-10		--
11	00h	Reserved

Attribute 184 : E2E Data Path Protection ECC Count from Flash to SATA Interface

Byte	Value	Description
0	184	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate.
3	64h	Attribute value (fixed at 100)
4	64h	Attribute value (worse value).
5-8		Number of E2E errors in direction of flash to SATA interface.
9-11	00h	Reserved

Attribute 185 : E2E Data Path Protection ECC Count from SATA Interface to Flash		
Byte	Value	Description
0	185	Attribute ID
1-2	001Ah	Flags – Advisory type, attribute value is updated during normal operation, attribute is an event count, attribute is an error rate.
3	64h	Attribute value (fixed at 100).
4	64h	Attribute value (worse value).
5-8		Number of E2E errors in direction of SATA interface to flash.
9-11	00h	Reserved

6.6. S.M.A.R.T. Read Attribute Thresholds

This command returns one sector of SMART attribute threshold data; the format is as follows:

Byte	Value	Description
0-1	0010h	SMART structure version
2-361		Attribute threshold entries 1-30 (12 bytes each)
362-379	00h	Reserved
380-510	00h	--
511		Checksum

The thresholds reported are as follows:

Byte	Value	Description
0	196	Attribute ID – Spare Block Count
1		Spare block count threshold
2-11	00h	Reserved

Byte	Value	Description
0	213	Attribute ID – Spare Block Count Worse Channel
1		Spare block count worst channel threshold
2-11	00h	Reserved

Byte	Value	Description
0	229	Attribute ID – Erase Count
1		Erase count threshold
2-11	00h	Reserved

Byte	Value	Description
0	203	Attribute ID – Total ECC Errors
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	204	Attribute ID – Correctable ECC Errors
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	199	Attribute ID – UDMA CRC Errors
1	00h	No threshold defined for this threshold.
2-11	00h	Reserved

Byte	Value	Description
0	232	Attribute ID – Total number of reads
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	12	Attribute ID – Power on count
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	241	Attribute ID – Total LBAs written
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	242	Attribute ID – Total LBAs read
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	214	Attribute ID – Anchor Block Status
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	215	Attribute ID – TRIM status
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	194	Attribute ID – Temperature status
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	184	Attribute ID – E2E Data Path Protection ECC Count from Flash to SATA Interface.
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	185	Attribute ID – E2E Data Path Protection ECC Count from SATA Interface to Flash
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	216	Attribute ID – Total Main Memory ECC Error Count
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

Byte	Value	Description
0	217	Attribute ID – Total Main Memory ECC Error Count in Firmware Memory
1	00h	No threshold defined for this attribute.
2-11	00h	Reserved

6.7. S.M.A.R.T. Return Status

Reports the drive reliability status. Values reported when a predicted defect has not been detected:

Cylinder Low register: 4Fh
Cylinder High register: C2h

Values reported when a predicted defect has been detected:

Cylinder Low register: F4h
Cylinder High register: 2Ch

6.8. S.M.A.R.T. Read Log

This command returns the data of the SMART log. When issuing this command, set the Sector Count register to the number of sectors to read and set the Sector Number register to the Log address. The Log addresses are defined as follows:

Address	Description
0x00	Log directory

Address	Description
0x80-0x9F	Host Vendor Specific logs
0xA1	SMART Remap data
0xA2	Reserved

The Log directory (address 0) returns 1 sector of data that shows the number of sectors for the defined Log addresses:

Byte	Value	Description
0-1	1	SMART logging version
2-3	1	Number of sectors in the SMART Error log summary
4-5	51	Number of sectors in the Comprehensive SMART Error log
6-7	16383	Number of sectors in the Extended Comprehensive SMART Error log
96-97	9	Identify Device data
256-319	16	Number of sectors in the logs at addresses 0x80-0x9F
320-321	4	Reserved
322-323	1	Number of sectors for SMART Log at address 0xA1
324-325	1	Number of sectors for SMART Log at address 0xA2

All other bytes in the Log Directory are zero.

The SMART Error Logs contain entries for internal flash errors or host transfer errors. If the corresponding host command for a flash error could not be determined, the command code field in the error entry is set to 0xF0.   For flash errors that do not correspond to a processed host command, the command code field is set to 0xFF.

The Host Vendor Specific Logs can be used by the host to store and retrieve arbitrary data. The SMART SMART Remap Data logs return the same data that is also returned by the SMART Read Remap Data command.

6.9.   S.M.A.R.T. Write Log

This command writes data of the SMART log. When issuing this command, set the Sector Count register to the number of sectors to write and set the Sector Number register to the Log address. Only the Host Vendor Specific logs can be written, all other logs are read only.

6.10. S.M.A.R.T. Read Remap Data

This command returns spare block information. When issuing this command, set the Sector Count register to 1. The information returned is the number of initial spare blocks available for remapping bad blcoks and the current number of spare blocks available for remapping bad blocks. The format is as follows:

Bytes	Description
0-31	Initial number of spare blocks for interleave units 0 to 15 (2 bytes per unit)
32-63	Current number of spare blocks for interleave units 0 to 15 (2 bytes per unit)
64-511	Reserved

Appendix A. Ordering Information

Model KCXFY-X00S

Where: X is drive capacities:
    1G ---------------- 1GB
    2G ---------------- 2GB
    4G ---------------- 4GB
    8G ---------------- 8GB
    16G ------------- 16GB
    32G ------------- 32GB
    64G ------------- 64GB

Where Y is temperature:
Blank --------------- Standard temperature (0° C to +70° C)
I --------------------- Extended temperature (-40° C to +85° C)

Example:

(1) 8GB CFast -- KC8GF-X00S
(2) 8GB CFast Extended Temp ------------------------------------ KC8GFI-X00S

Appendix B.Technical Support Services

B.1.Direct Cactus Technologies® Technical Support

Email: tech@cactus-tech.com

Appendix C.Cactus Technologies® Worldwide Sales Offices

Email: sales@cactus-tech.com

Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited to customers of our products.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Industrial Grade Flash Storage Products. Cactus Technologies®, at its sole option, will repair, replace or refund the purchase price of the defective product. Cactus Technologies® guarantees our products meet all specifications detailed in our product manuals. Although Cactus Technologies® products are designed to withstand harsh environments and have the highest specifications in the industry, they are not warranted to never have failure and Cactus Technologies® does not warranty against incidental or consequential damages. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or backup features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing, replacing or refunding the purchase price the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs. Cactus Technologies® Limited may repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department (tech@cactus-tech.com) with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number with shipping instructions.