



# **Industrial Grade CF Card -603 Series Product Manual**

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# 1. Introduction To Cactus Technologies® Industrial Grade CF -603 Series Products

## Features:

- Solid state design with no moving parts
- Industry standard CF Type I form factor
- Supports TrueIDE Mode
- Supports ATA PIO Modes 0-6 in TrueIDE Mode
- Supports MultiWord DMA Modes 0-4 in TrueIDE Mode
- Supports UDMA Modes 0-5 in TrueIDE Mode
- Supports ATA S.M.A.R.T. Feature Set
- Supports ATA Security Feature Set
- Enhanced error correction, < 1 error in  $10^{14}$  bits read
- Intelligent power management to reduce power consumption
- Voltage support: 5.0V

## Overview:

Cactus Technologies® CompactFlash Memory Card (CF) is a high capacity solid-state flash memory product that complies with the Personal Computer Memory Card International Association (PCMCIA) ATA (PC Card ATA) standard. It also supports True IDE Mode, which is electrically compatible with an IDE disk drive. CompactFlash Memory Cards provide up to 64GB of formatted storage capacity in the CF Type I form factor.

Cactus Technologies® Industrial Grade CF products use high quality SLC flash memory from Kioxia Corporation (formerly Toshiba Corporation). In addition, it includes an on-card intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control.

## 1.1. Supported Standards

Cactus Technologies® CompactFlash Memory Cards are fully electrically compatible with the following specifications:

- *PCMCIA PC Card Standard v8.0*
- *PCMCIA PC Card ATA Specification*
- *CompactFlash Specification 6.1*
- ATA7 Specification published by ANSI: X3.221 AT Attachment Interface for Disk Drives

## 1.2. Product Features

Cactus Technologies® Industrial Compact Flash Cards contain a high level, intelligent controller. This intelligent controller provides many capabilities not found in other types of memory cards. These capabilities include the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

### 1.2.1. Host and Technology Independence

Cactus Technologies® Industrial CF Cards appears as a standard ATA disk drive to the host system. The card utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the card as per the ATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the card. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies® Industrial CF products today will continue to work with future Cactus Technologies® Industrial CF cards built with new flash technology without having to update or change host software.

### 1.2.2. Defect and Error Management

Cactus Technologies® Industrial CF cards contain a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® Industrial CF cards is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the card has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® Industrial CF cards unparalleled reliability.

### **1.2.3. Intelligent Power Management**

Cactus Technologies® Industrial CF cards employ sophisticated power management algorithms to conserve power. Upon completion of a command, the card will automatically enter sleep mode if no further commands are received. In most situations, the card will be in sleep mode except when the host is accessing it, thus conserving power. The delay from command completion to entering sleep mode can be adjusted.

When the card is in sleep mode, any command issued to the card will cause it to exit sleep and respond.

### **1.2.4. Power Supply Requirements**

This product will operate at a voltage range of 5.00 volts  $\pm$  10%.

## 2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

### 2.1. System Environmental Specifications

**Table 2-1. Environmental Specifications**

		Cactus Technologies® -603 CF Products
Temperature	Operating:	0° C to +70° C (Standard) -40° C to +85° C (Extended)
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Acoustic Noise		0 dB
Vibration	Non-Operating:	16.4 G MIL-STD-810F Method 514.5, Procedure 1
Shock	Operating & Non-Operating:	50 G MIL-STD_810F Method 516.5, Procedure 1
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

### 2.2. System Power Requirements

**Table 2-2. Power Requirements**

		Cactus Technologies® -603 CF Products									
<b>DC Input Voltage(VCC) 100 mV max. ripple (p-p)</b>		5.0V ±10%									
		128M	256M	512M	1G	2G	4G	8G	16G	32G	64G
<b>(Maximum Average Value) mA See Notes.</b>	Sleep:	4	4	4	4	4	4	4	4	4	4
	Reading:	61	65	67	69	101	110	107	111	122	135
	Writing:	52	57	61	63	90	92	90	83	89	98

**NOTES:** All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all card inputs are static CMOS levels and in a “Not Busy” operating state.



## 2.3. System Performance

All performance numbers are typical values assuming the card controller is in the default (i.e., fastest) mode.

**Table 2-3. Performance**

	128M	256M	512M	1G	2G	4G	8G	16G	32G	64G
<b>Seq. Read Transfer Rate (MBytes/s)</b>	24	29	32	32	61	65	63	64	65	64
<b>Seq. Write Transfer Rate (MBytes/s)</b>	5	11	20	20	30	41	37	44	44	44
<b>Random 4K Write (Mbytes/s)</b>	22	24	26	26	44	36	38	37	37	37
<b>Random 4K Read (MBytes/s)</b>	2	5	9	9	13	16	16	15	16	17

\* Please note that for maximum performance in TrueIDE UDMA modes, proper termination and PCB layout guidelines as described in the ATA specifications must be followed to minimize signal integrity problems.

## 2.4. System Reliability

**Table 2-4. Reliability**

Data Reliability	< 1 non-recoverable error in 10 <sup>14</sup> bits READ
Endurance (estimated TBW):	128MB: 7.68TB 256MB: 15.36TB 512MB: 30.72TB 1GB: 60TB 2GB: 120TB 4GB: 240TB 8GB: 480TB 16GB: 960TB 32GB: 1920TB 64GB: 3840TB

**Note: TBW estimation is based on a workload of large block sequential write at room temperature. A workload of random, small block writes can significantly reduce TBW.**

## 2.5. Physical Specifications

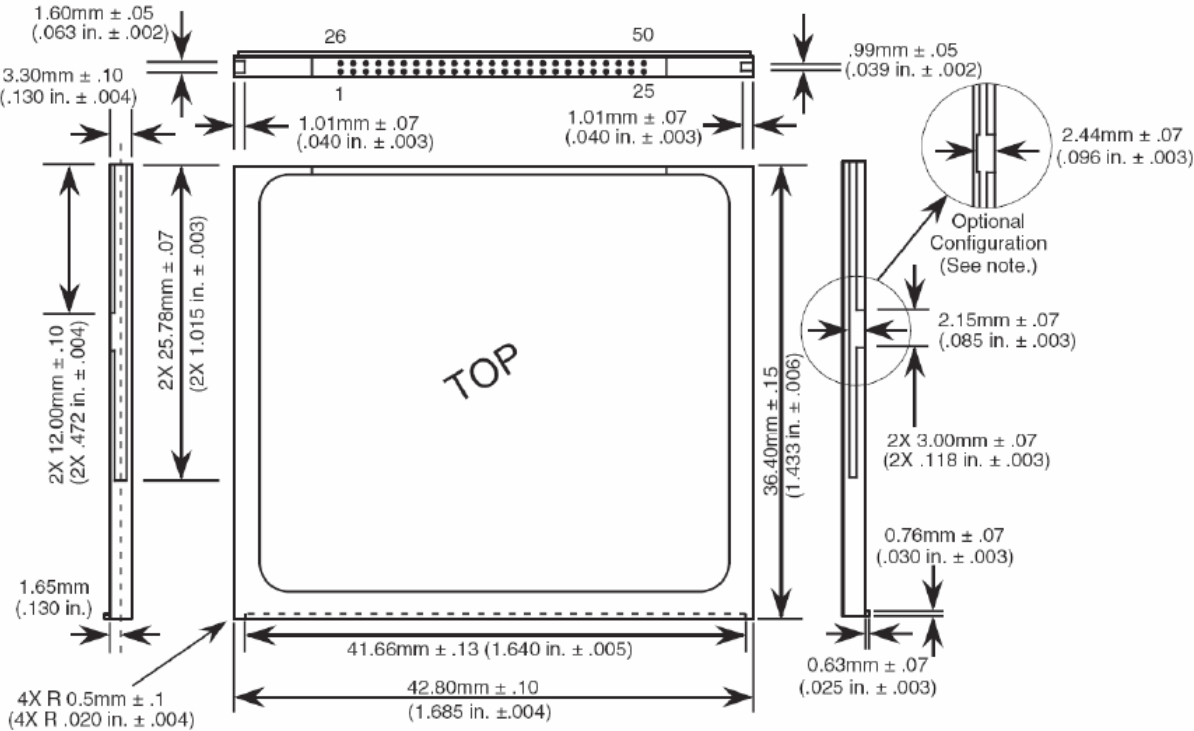
The following sections provide the physical specifications for Cactus Technologies® Industrial CompactFlash products.

## 2.5.1. CompactFlash Physical Specifications

Refer to Table 2-5 and see Figures 2-1 and 2-2 for CompactFlash Memory Card physical specifications and dimensions.

**Table 2-5. CompactFlash Physical Specifications**

Weight:	11.4 g (.40 oz) typical, 14.2 g (.50 oz) maximum
Length:	36.40 ± 0.15 mm (1.433 ± .006 in)
Width:	42.80 ± 0.10 mm (1.685 ± .004 in)
Thickness:	3.3 mm ± 0.10 mm (.130 ± .004 in) (Excluding Lip)



Note: The optional notched configuration was shown in the CF Specification Rev. 1.0. In specification Rev. 1.2, the notch was removed for ease of tooling. This optional configuration can be used but it is not recommended.

**Figure 2-1. CompactFlash Memory Card Dimensions**

## **2.6. Capacity Specifications**

Cactus Technologies® offers CompactFlash products in the following capacities:

128M, 256M, 512M, 1G, 2G, 4G, 8G, 16G, 32G and 64G

## 3. Interface Description

The following sections provide detailed information on the Cactus Technologies® Industrial CompactFlash card interface.

### 3.1. CF Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 3-6. Low active signals have a “-” prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 to 3.3.4 define the DC characteristics for all input and output type structures.

**Table 3-6. CompactFlash Pin Assignments and Pin Type**

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode <sup>4</sup>		
Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10 <sup>2</sup>	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09 <sup>2</sup>	I
11	A08	I	11	A08	I	11	A08 <sup>2</sup>	I
12	A07	I	12	A07	I	12	A07 <sup>2</sup>	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06 <sup>2</sup>	I
15	A05	I	15	A05	I	15	A05 <sup>2</sup>	I
16	A04	I	16	A04	I	16	A04 <sup>2</sup>	I
17	A03	I	17	A03	I	17	A03 <sup>2</sup>	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	23	D02	I/O	23	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11 <sup>1</sup>	I/O	27	D11 <sup>1</sup>	I/O	27	D11 <sup>1</sup>	I/O
28	D12 <sup>1</sup>	I/O	28	D12 <sup>1</sup>	I/O	28	D12 <sup>1</sup>	I/O
29	D13 <sup>1</sup>	I/O	29	D13 <sup>1</sup>	I/O	29	D13 <sup>1</sup>	I/O
30	D14 <sup>1</sup>	I/O	30	D14 <sup>1</sup>	I/O	30	D14 <sup>1</sup>	I/O
31	D15 <sup>1</sup>	I/O	31	D15 <sup>1</sup>	I/O	31	D15 <sup>1</sup>	I/O
32	-CE2 <sup>1</sup>	I	32	-CE2 <sup>1</sup>	I	32	-CS1 <sup>1</sup>	I
33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD HSTROBE <sup>10</sup> HDMARDY <sup>11</sup>	I	34	-IORD HSTROBE <sup>10</sup> HDMARDY <sup>11</sup>	I	34	-IORD <sup>7</sup> HSTROBE <sup>8</sup> HDMARDY <sup>9</sup>	I
35	-IOWR STOP <sup>10,11</sup>	I	35	-IOWR STOP <sup>10,11</sup>	I	35	-IOWR <sup>7</sup> STOP <sup>8,9</sup>	I
36	-WE	I	36	-WE	I	36	-WE <sup>3</sup>	I

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode <sup>4</sup>		
37	RDY/BSY	O	37	IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL <sup>5</sup>	I	39	-CSEL <sup>5</sup>	I	39	-CSEL	I
40	-VS2	I/O	40	-VS2	I/O	40	-VS2	I/O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT DDMARDY <sup>10</sup> DSTROBE <sup>11</sup>	O	42	-WAIT DDMARDY <sup>10</sup> DSTROBE <sup>11</sup>	O	42	IORDY <sup>7</sup> DDMARDY <sup>8</sup> DSTROBE <sup>9</sup>	O <sup>13</sup>
43	-INPACK -DMARQ <sup>12</sup>	O	43	-INPACK -DMARQ <sup>12</sup>	O	43	DMARQ	O
44	-REG -DMACK <sup>12</sup>	I	44	-REG -DMACK <sup>12</sup>	I	44	-DMACK <sup>6</sup>	I
45	BVD2	I/O	45	-SPKR	I/O	45	-DASP	I/O
46	BVD1	I/O	46	-STSCHG	I/O	46	-PDIAG	I/O
47	D08 <sup>1</sup>	I/O	47	D08 <sup>1</sup>	I/O	47	D08 <sup>1</sup>	I/O
48	D09 <sup>1</sup>	I/O	48	D09 <sup>1</sup>	I/O	48	D09 <sup>1</sup>	I/O
49	D10 <sup>1</sup>	I/O	49	D10 <sup>1</sup>	I/O	49	D10 <sup>1</sup>	I/O
50	GND		50	GND		50	GND	

**NOTE:**

1. These signals are required only for 16-bit access and not required when installed in 8-bit systems. For lowest power dissipation, leave these signals open.
2. Should be grounded by the host.
3. Should be tied to VCC by the host.
4. This mode is mandatory for CompactFlash cards.
5. Do not leave this signal floating.
6. If DMA operation is not used, host shall tie this signal high. Devices that do not support DMA shall ignore this signal.
7. Signal usage when UDMA protocol is active.
8. Signal usage when UDMA write protocol is active.
9. Signal usage when UDMA read protocol is active.
10. Signal usage when UDMA write protocol is active.
11. Signal usage when UDMA read protocol is active.
12. Signal usage when UDMA protocol is active.
13. Signal is totem pole output when UDMA protocol is active in TrueIDE mode, otherwise, it is open drain.

## 3.2. Signal Description

Cactus Technologies® Industrial CompactFlash products can be configured to operate in either I/O mode or memory mode as per *PCMCIA Specification*. The configuration of the CompactFlash cards are controlled using the standard PCMCIA configuration registers starting at address 200h in the Attribute Memory space of the CompactFlash Memory Card. Cactus Technologies® Industrial CompactFlash cards also supports a TrueIDE mode. This mode is entered by grounding the -OE pin on power up.

Table 3-7 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the CompactFlash Memory Card sources are outputs. The CompactFlash Card logic levels conform to those specified in the *PCMCIA Specification*. See Section 3.3 for definitions of Input and Output type.

**Table 3-7. Signal Description**

Signal Name	Dir.	Description
A10—A0 (CF Card Memory Mode)	I	These address lines along with the -REG signal are used to select the following: The I/O port address registers within the CompactFlash Card, the memory mapped port address registers within the card, a byte in the card's information structure and its configuration control and status registers.
A10—A0 (CF Card I/O Mode)		This signal is the same as the CF Card Memory Mode signal.
A2—A0 (True IDE Mode) A10—A3 (True IDE Mode)	I	In True IDE Mode only A[2:0] is used to select the one of eight registers in the Task File.  In True IDE Mode these remaining address lines should be grounded by the host.
BVD1 (CF Card Memory Mode)	I/O	This signal is asserted high as the BVD1 signal since a battery is not used with this product.
-STSCHG (CF Card I/O Mode) Status Changed		This signal is asserted low to alert the host to changes in the RDY/-BSY and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register.
-PDIAG (True IDE Mode)		In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
BVD2 (CF Card Memory Mode)	I/O	This output line is always driven to a high state in Memory Mode since a battery is not required for this product.
-SPKR (CF Card I/O Mode)		This output line is always driven to a high state in I/O Mode since this product does not support the audio function.
-DASP (True IDE Mode)		In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CD1, -CD2 (CF Card Memory Mode)	O	These Card Detect pins are connected to ground on the CompactFlash Card. They are used by the host to determine if the card is fully inserted into its socket.
-CD1, -CD2 (CF Card I/O Mode)		This signal is the same for all modes.
-CD1, -CD2 (True IDE Mode)		This signal is the same for all modes.
-CE1, -CE2 (CF Card Memory Mode) Card Enable	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. -CE2 always accesses the odd byte of the word. -CE1 accesses the even byte or the Odd byte of the word depending on A0 and -CE2. A multiplexing scheme based on A0, -CE1, and -CE2 allows 8 bit hosts to access all data on D0-D7. See Tables 3-11, 3-12, 3-15, and 3-16.
-CE1, -CE2 (CF Card I/O Mode) Card Enable		This signal is the same as the CF Card Memory Mode signal.
-CS0, -CS1 (True IDE Mode)		In the True IDE Mode -CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL (CF Card Memory Mode)	I	This signal is not used for this mode.
-CSEL (CF Card I/O Mode)		This signal is not used for this mode.
-CSEL (True IDE Mode)		This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15—D00 (CF Card Memory Mode)	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word.
D15—D00 (CF Card I/O Mode)		These signals are the same as the CF Card Memory Mode signal.
D15—D00 (True IDE Mode)		In True IDE Mode all Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bits using D00-D15.
GND (CF Card Memory Mode)	--	Ground.

Signal Name	Dir.	Description
GND (CF Card I/O Mode)		This signal is the same for all modes.
GND (True IDE Mode)		This signal is the same for all modes.
-INPACK (CF Card Memory Mode; non UDMA)	O	This signal is not used in this mode.
-INPACK (CF Card I/O Mode, non UDMA) Input Acknowledge		The Input Acknowledge signal is asserted by the CompactFlash Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the card and the CPU.
DMARQ (True IDE Mode, Memory Mode w/ UDMA, I/O mode w/ UDMA)		In all modes when UDMA is supported and active, this pin is an output from the card to request DMA mode transfer.
-IORD (CF Card Memory Mode, non UDMA)	I	This signal is not used in this mode.
-IORD (CF Card I/O Mode, non UDMA)		This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash Card when the card is configured to use the I/O interface.
-IORD (True IDE Mode, UDMA not active) -HDMARDY (all modes, UDMA read) HSTROBE (all modes, UDMA write)		In True IDE Mode, when UDMA protocol is not active, this signal has the same function as in CF Card I/O Mode.  In all modes, when UDMA read protocol is active, this signal is asserted by the host to indicate that it is ready to receive data-in bursts.  In all modes, when UDMA write protocol is active, this signal is the data out strobe sent by the host. Data is latched by the device on both rising and falling edges of this signal.
-IOWR (CF Card Memory Mode, non UDMA) -IOWR (CF Card I/O Mode, non UDMA) -IOWR (True IDE Mode, UDMA not active) STOP (all modes, UDMA active)	I	This signal is not used in this mode.  The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the CompactFlash controller registers when the card is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge).  In True IDE Mode, when UDMA protocol is not active, this signal has the same function as in CF Card I/O Mode.  In all modes, when UDMA protocol is active, host asserts this signal to terminate the UDMA transfer.
-OE (CF Card Memory Mode) -OE (CF Card I/O Mode) -ATA SEL (True IDE Mode)	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Card in Memory Mode and to read the CIS and configuration registers.  In CF Card I/O Mode, this signal is used to read the CIS and configuration registers.  To enable True IDE Mode this input should be grounded by the host.

Signal Name	Dir.	Description
RDY/-BSY (CF Card Memory Mode)	O	In Memory Mode this signal is set high when the CompactFlash Card is ready to accept a new data transfer operation and held low when the card is busy. The Host memory card socket must provide a pull-up resistor.  At power up and at Reset, the RDY/-BSY signal is held low (busy) until the CompactFlash Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Card during this time. The RDY/-BSY signal is held high (disabled from being busy) whenever the following condition is true: The CompactFlash Card has been powered up with +RESET continuously disconnected or asserted.
-IREQ (CF Card I/O Mode)		I/O Operation—After the CompactFlash Card has been configured for I/O operation, this signal is used as -Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE Mode)		In True IDE Mode, this signal is the active high Interrupt Request to the host.
-REG (CF Card Memory Mode, non UDMA) Attribute Memory Select	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory.  The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
-REG (CF Card I/O Mode, non UDMA)		In all modes when UDMA is active, this is an input from the host to signal that the DMA request from the device has been acknowledged.
-DMACK (all modes, UDMA active)		
RESET (CF Card Memory Mode)	I	When the pin is high, this signal resets the CompactFlash Card. The card is Reset only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
RESET (CF Card I/O Mode)		This signal is the same as the CF Card Memory Mode signal.
-RESET (True IDE Mode)		In the True IDE Mode this input pin is the active low hardware reset from the host.
VCC (CF Card Memory Mode)	--	+5 V, +3.3 V power.
VCC (CF Card I/O Mode)		This signal is the same for all modes.
VCC (True IDE Mode)		This signal is the same for all modes.
-VS1 -VS2 (CF Card Memory Mode)	O	Voltage Sense Signals. -VS1 is grounded so that the CompactFlash Card CIS can be read at 3.3 volts and -VS2 is open and reserved by CF Card for a secondary voltage.
-VS1 -VS2 (CF Card I/O Mode)		This signal is the same for all modes.
-VS1 -VS2 (True IDE Mode)		This signal is the same for all modes.



Signal Name	Dir.	Description
-WAIT (CF Card Memory Mode, non UDMA) -WAIT (CF Card I/O Mode, non UDMA) -IORDY (True IDE Mode, UDMA not active) -DDMARDY (all modes, UDMA write active) DSTROBE (all modes, UDMA read active)	O	The –WAIT signal is driven by the CompactFlash Card to signal to the host to delay completion of the memory cycle in progress.  The –WAIT signal is driven by the CompactFlash Card to signal to the host to delay completion of the I/O cycle in progress.  In TrueIDE Mode, when UDMA protocol is not active, this signal is driven by the device to extend the I/O cycle in progress.  In all modes, when UDMA write protocol is active, this signal is asserted by the device to indicate that it is ready to receive a data out burst.  In all modes, when UDMA read protocol is active, this signal is the data strobe sent by the device to the host. The host latches data on both the rising and falling edges of this signal.
-WE (CF Card Memory Mode) -WE (CF Card I/O Mode) Reserved (True IDE Mode)	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.  In CF Card I/O Mode, this signal is used for writing the configuration registers.  In True IDE Mode this input signal is not used and should be connected to VCC by the host.
WP (CF Card Memory Mode) Write Protect -IOIS16 (CF Card I/O Mode) -IOCS16 (True IDE Mode)	O	Memory Mode—The CompactFlash Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.  I/O Operation—When the CompactFlash Card is configured for I/O Operation, Pin 24 is used for the -I/O Selected is 16 Bit Port (-IOIS16) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port.  In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

### 3.3. Electrical Specification

The following table defines all D.C. Characteristics for the CompactFlash Memory Card Series. Unless otherwise stated, conditions are:

$$V_{cc} = 5V \pm 10\%$$

$$T_a = -40^{\circ}C \text{ to } 85^{\circ}C$$

#### 3.3.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	T <sub>s</sub>	-55	+100	°C
Operating Temperature	T <sub>A</sub>	-40	+85	°C
V <sub>cc</sub> with respect to GND	V <sub>cc</sub>	-0.3	6.5	V

### 3.3.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	V <sub>in</sub>	-0.5	V <sub>CC</sub> + 0.5	V
Output Voltage	V <sub>out</sub>	-0.3	V <sub>CC</sub> + 0.3	V
Input Leakage Current	I <sub>LI</sub>	-10	10	uA
Output Leakage Current	I <sub>LO</sub>	-10	10	uA
Input/Output Capacitance	C <sub>I</sub> /C <sub>O</sub>		10	pF
Operating Current	I <sub>CC</sub>			mA
Idle			4	
Active			140	

### 3.3.3. AC Characteristics

Cactus Technologies® CF Cards meet all the timing requirements as specified in *CompactFlash Specification 6.1* and *PCMCIA PC Card Standard v8.0*. Please refer to those documents for details on interface AC timing diagrams and specifications.

## 3.4. Card Configuration

The CompactFlash Memory Cards are identified by information in the Card Information Structure (CIS). The entries in Table 3-8 and Table 3-9 show how to access the various registers and address spaces in the memory cards.

**Table 3-8. Registers and Memory Space Decoding**

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED SPACE
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 Bit D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 Bit D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 Bit D15-D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 Bit D15-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

**Table 3-9. Configuration Registers Decoding**

-CE2	-CE1	-REG	-OE	-WE	A10	A9	A8-A4	A3	A2	A1	A0	SELECTED REGISTER
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

**NOTE:** The location of the card configuration registers should always be read from the CIS since these locations may vary in future products. No writes should be performed to the CompactFlash Memory Card attribute memory except to the card configuration register addresses. All other attribute memory locations are reserved.

### 3.4.1. Attribute Memory Function

Attribute memory is a space where CompactFlash Memory Card CIS and configurations registers are stored, and is limited to 8-bit wide accesses only at even addresses.

As in the Main Memory Read functions, the signals -CE1 and -CE2 control the even-byte and odd-byte address, but only the even-byte data is valid during the Attribute Memory access. Refer to Table 3-10 for signal states and bus validity for the Attribute Memory function.

**Table 3-10. Attribute Memory Function**

Function Mode	-REG	-CE2	-CE1	A9	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	L	H	L	L	L	L	H	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	L	H	L	L	L	H	L	Do not care	Even Byte
Read Byte Access Configuration (8 bits)	L	H	L	H	L	L	H	High Z	Even Byte
Write Byte Access Configuration (8 bits)	L	H	L	H	L	H	L	Do not care	Even Byte
Read Word Access CIS (16 bits)	L	L	L	L	X	L	H	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	L	L	L	L	X	H	L	Do not care	Even Byte
Read Word Access Configuration (16 bits)	L	L	L	H	X	L	H	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	L	L	L	H	X	H	L	Do not care	Even Byte

**NOTE:** The -CE signal or both the -OE signal and the -WE signal must be de-asserted between consecutive cycle operations.

### 3.4.2. Configuration Option Register (Address 200h in Attribute Memory)

The Configuration Option Register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash Memory Card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

**SRESET** Soft Reset—Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash Memory Card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the +RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash Memory Card in the same un-configured, Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PC Card Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control Register.

**LevIREQ** This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse Mode is selected. Set to zero (0) by Reset.

**Conf5—Conf0** Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the CompactFlash Memory Card as shown below.

**NOTE:** Conf5 and Conf4 are reserved and must be written as zero (0).

**Table 3-11. Card Configurations**

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, Any 16 byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	I/O Mapped, 170-177/376-377

### 3.4.3. Card Configuration and Status Register (Address 202h in Attribute Memory)

The Card Configuration and Status Register contain information about the Card's condition.

**Table 3-12. Card Configuration and Status Register Organization**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOis8	0	0	PwrDwn	0	0

**Changed** Indicates that one or both of the Pin Replacement register CRdy, or CWProt bits are set to one (1). When the Changed bit is set, -STSCHG Pin 46 is held low if the SigChg bit is a One (1) and the CompactFlash Memory Card is configured for the I/O interface.

**SigChg** This bit is set and reset by the host to enable and disable a state-change "signal" from the Status Register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (-STSCHG) signal will be held high while the CompactFlash Memory Card is configured for I/O.

**IOis8** The host sets this bit to a one (1) if the CompactFlash Memory Card is to be configured in an 8-bit I/O mode. The CompactFlash Card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

**PwrDwn** This bit indicates whether the host requests the CompactFlash Memory Card to be in the power saving or active mode. When the bit is one (1), the CompactFlash Card enters a power down mode. When zero (0), the host is requesting the CompactFlash Card to enter the active mode. The PC Card Rdy/-Bsy value becomes BUSY when this bit is changed. Rdy/-Bsy will not become Ready until the power state requested has been entered. The CompactFlash Card automatically powers down when it is idle and powers back up when it receives a command.

**Int** This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition that caused the interrupt request has been serviced. If interrupts are disabled by the -IEN bit in the Device Control Register, this bit is a zero (0).

### 3.4.4. Pin Replacement Register (Address 204h in Attribute Memory)

**Table 3-13. Pin Replacement Register**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRdy/-Bsy	CWProt	1	1	RRdy/-Bsy	RWProt
Write	0	0	CRdy/-Bsy	CWProt	0	0	MRdy/-Bsy	MWProt

**CRdy/-Bsy** This bit is set to one (1) when the bit RRdy/-Bsy changes state. This bit can also be written by the host.

**CWProt** This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

**RRdy/-Bsy** This bit is used to determine the internal state of the Rdy/-Bsy signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

**RWProt** This bit is always zero (0) since the CompactFlash Memory Card does not have a Write Protect switch. When written, this bit acts as a mask for writing the corresponding bit CWProt.

**MRdy/-Bsy** This bit acts as a mask for writing the corresponding bit CRdy/-Bsy.

**MWProt** This bit when written acts as a mask for writing the corresponding bit CWProt.

**Table 3-14. Pin Replacement Changed Bit/Mask Bit Values**

Initial Value of (C) Status	Written by Host		Final "C" Bit	Comments
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by Host
X	1	1	1	Set by Host

### 3.4.5. Socket and Copy Register (Address 206h in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index Register.

**Table 3-15. Socket and Copy Register Organization**

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive # (0)	X	X	X	X

**Reserved** This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

**Drive #** This bit indicates the drive number of the card if twin card configuration is supported.  
**X** The socket number is ignored by the CompactFlash Memory Card.

### 3.5. I/O Transfer Function

The I/O transfer to or from the CompactFlash Memory Card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal -IOIS16 is asserted by the CompactFlash Card. Otherwise, the -IOIS16 signal is de-asserted. When a 16-bit transfer is attempted, and the -IOIS16 signal is not asserted by the CompactFlash Card, the system must generate a pair of 8-bit references to access the word's even byte and odd byte. The CompactFlash Card permits both 8- and 16-bit accesses to all of its I/O addresses, so -IOIS16 is asserted for all addresses to which the CompactFlash Card responds (refer to Table 3-16).

**Table 3-16. I/O Function**

Function Code	-REG	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Input Access (8 bits)	L	H	L	L	L	H	High Z	Even-Byte
	L	H	L	H	L	H	High Z	Odd-Byte
Byte Output Access (8 bits)	L	H	L	L	H	L	Do not care	Even-Byte
	L	H	L	H	H	L	Do not care	Odd-Byte
Word Input Access (16 bits)	L	L	L	L	L	H	Odd-Byte	Even-Byte
Word Output Access (16 bits)	L	L	L	L	H	L	Odd-Byte	Even-Byte
I/O Read Inhibit	H	X	X	X	L	H	Do not care	Do not care
I/O Write Inhibit	H	X	X	X	H	L	High Z	High Z
High Byte Input Only (8 bits)	L	L	H	X	L	H	Odd-Byte	High Z
High Byte Output Only (8 bits)	L	L	H	X	H	L	Odd-Byte	Do not care

### 3.6. Common Memory Transfer Function

The Common Memory transfer to or from the CompactFlash card can be either 8 or 16 bits. The CompactFlash cards permit both 8- and 16-bit accesses to all of its Common addresses (refer to Table 3-17).

**Table 3-17. Common Memory Function**

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Standby Mode	X	H	H	X	X	X	High Z	High Z
Byte Read Access (8 bits)	H	H	L	L	L	H	High Z	Even-Byte
	H	H	L	H	L	H	High Z	Odd-Byte
Byte Write Access (8 bits)	H	H	L	L	H	L	Do not care	Even-Byte
	H	H	L	H	H	L	Do not care	Odd-Byte
Word Read Access (16 bits)	H	L	L	X	L	H	Odd-Byte	Even-Byte
Word Write Access (16 bits)	H	L	L	X	H	L	Odd-Byte	Even-Byte

Function Code	-REG	-CE2	-CE1	A0	-OE	-WE	D15-D8	D7-D0
Odd Byte Read Only (8 bits)	H	L	H	X	L	H	Odd-Byte	High Z
Odd Byte Write Only (8 bits)	H	L	H	X	H	L	Odd-Byte	Do not care

### 3.7. True IDE Mode I/O Transfer Function

The CompactFlash card can be configured in a True IDE Mode of operation. This CompactFlash card is configured in this mode only when the -OE input signal is grounded by the host when power is applied to the card. In True IDE Mode, the CF Card protocol and configuration are disabled and only I/O operations to the Task File and Data Register are allowed. In addition, No Memory or Attribute Registers are accessible to the host.

**NOTE:** Removing and reinserting the CompactFlash Memory Card while the host computer's power is on will reconfigure the CompactFlash Card to PC Card ATA mode from the original True IDE Mode. To configure the CompactFlash Card in True IDE Mode, the 50-pin socket must be power cycled with the CompactFlash Card inserted and -OE (output enable) grounded by the host.

Table 3-18 defines the function of the operations for the True IDE Mode.

**Table 3-18. IDE Mode I/O Function**

Function Code	-CE2	-CE1	A0	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Do not care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Do not care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

## 4. ATA Drive Register Set Definition And Protocol

The CompactFlash Memory Card can be configured as a high performance I/O device through the following ways:

- Standard PC-AT disk I/O address spaces 1F0h-1F7h, 3F6h-3F7h (primary); 170h-177h, 376h-377h (secondary) with IRQ 14 (or other available IRQ).
- Any system decoded 16-byte I/O block using any available IRQ.
- Memory space.

The communication to or from the CompactFlash Memory Card is done using the Task File registers, which provide all the necessary registers for control and status information. The PC Card interface connects peripherals to the host using four register mapping methods. Table 4-19 is a detailed description of these methods.

**Table 4-19. I/O Configurations**

Standard Configurations				
Config Index	IO or Memory	Address	Drive #	Description
0	Memory	0-F, 400-7FF	0	Memory Mapped
1	I/O	XX0-XXF	0	I/O Mapped 16 Contiguous Registers
2	I/O	1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
2	I/O	1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
3	I/O	170-177, 376-377	0	Secondary I/O Mapped Drive 0
3	I/O	170-177, 376-377	1	Secondary I/O Mapped Drive 1

## 4.1. I/O Primary and Secondary Address Configurations

**Table 4-20. Primary and Secondary I/O Decoding**

-REG	A9-A4	A3	A2	A1	A0	-IORD=0	-IOWR=0	Note
0	1F(17)	0	0	0	0	Even RD Data	Even WR Data	1, 2
0	1F(17)	0	0	0	1	Error Register	Features	1
0	1F(17)	0	0	1	0	Sector Count	Sector Count	
0	1F(17)	0	0	1	1	Sector No.	Sector No.	
0	1F(17)	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)	0	1	1	1	Status	Command	
0	3F(37)	0	1	1	0	Alt Status	Device Control	
0	3F(37)	0	1	1	1	Drive Address	Reserved	

- Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
- A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

## 4.2. Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash Memory Card, the registers are accessed in the block of I/O space decoded by the system in Table 4-21.

**Table 4-21. Contiguous I/O Decoding**

-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	



-REG	A3	A2	A1	A0	Offset	-IORD=0	-IOWR=0	Notes
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

**NOTES:** 1. Register 0 is accessed with -CE1 low and -CE2 low (and A0 = Do not care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.

A byte access to register 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.

Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Address lines that are not indicated are ignored by the CompactFlash Memory Card for accessing all the registers in this table.

## 4.3. Memory Mapped Addressing

When the CompactFlash Memory Card registers are accessed via memory references, the registers appear in the common memory space window: 0-2K bytes as shown in Table 4-22.

**Table 4-22. Memory Mapped Decoding**

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3

-REG	A10	A9-A4	A3	A2	A1	A0	Offset	-OE=0	-WE=0	Notes
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

**NOTES:**1. Register 0 is accessed with -CE1 low and -CE2 low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with -CE1 low and -CE2 high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with -CE1 low, the first byte to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.  
A byte access to address 0 with -CE1 high and -CE2 low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.

Register 8 is equivalent to register 0, while register 9 accesses the odd byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred odd byte then even byte.

Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.

3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PC Card socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the CompactFlash Memory Card.

## 4.4. True IDE Mode Addressing

When the CompactFlash Memory Card is configured in the True IDE Mode the I/O decoding is as listed in Table 4-23.

**Table 4-23. True IDE Mode I/O Decoding**

-CE2	-CE1	A2	A1	A0	-IOR=0	-IOWR=0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

## 4.5. ATA Registers

**NOTE:** In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when -CE1 is high and -CE2 is low unless -IOIS16 is high (not asserted) and an I/O cycle is being performed.

### 4.5.1. Data Register (Address—1F0[170]; Offset 0, 8, 9)

The Data Register is a 16-bit register, and it is used to transfer data blocks between the CF card data buffer and the Host. This register overlaps the Error Register. Table 4-24 describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

**NOTE:** Because of the overlapped registers, access to the 1F1, 171 or offset 1 are not defined for word (-CE2 = 0 and -CE1 = 0) operations. Accesses to these locations are treated as accesses to the Word Data Register. The duplicated registers at offsets 8, 9 and Dh have no restrictions on the operations that can be performed by the socket.

**Table 4-24. Data Register**

Data Register	CE2-	CE1-	A0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	D15-D0
Even Data Register	1	0	0	0,8	D7-D0
Odd Data Register	1	0	1	9	D7-D0
Odd Data Register	0	1	X	8,9	D15-D8
Error/Feature Register	1	0	1	1, Dh	D7-D0
Error/Feature Register	0	1	X	1	D15-D8
Error/Feature Register	0	0	X	Dh	D15-D8

### 4.5.2. Error Register (Address—1F1[171]; Offset 1, 0Dh Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with -CE2 low and -CE1 high.

**Bit 7 (BBK)** This bit is set when a Bad Block is detected.

**Bit 6 (UNC)** This bit is set when an Uncorrectable Error is encountered.

**Bit 5** This bit is 0.

**Bit 4 (IDNF)** The requested sector ID is in error or cannot be found.

**Bit 3** This bit is 0.

**Bit 2 (Abort)** This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

**Bit 1** This bit is 0.

**Bit 0 (AMNF)** This bit is set in case of a general error.

### 4.5.3. Feature Register (Address—1F1[171]; Offset 1, 0Dh Write Only)

This register provides information regarding features of the CF card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with -CE2 low and -CE1 high (except in True IDE Mode operation).

### 4.5.4. Sector Count Register (Address—1F2[172]; Offset 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash Memory Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

### 4.5.5. Sector Number (LBA 7-0) Register (Address—1F3[173]; Offset 3)

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash Memory Card data access for the subsequent command.

### 4.5.6. Cylinder Low (LBA 15-8) Register (Address—1F4[174]; Offset 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

### 4.5.7. Cylinder High (LBA 23-16) Register (Address—1F5[175]; Offset 5)

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

### 4.5.8. Drive/Head (LBA 27-24) Register (Address 1F6[176]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

**Bit 7** This bit is set to 1.

**Bit 6** LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:

LBA07-LBA00: Sector Number Register D7-D0.

LBA15-LBA08: Cylinder Low Register D7-D0.

LBA23-LBA16: Cylinder High Register D7-D0.

LBA27-LBA24: Drive/Head Register bits HS3-HS0.

**Bit 5** This bit is set to 1.

- Bit 4 (DRV)** This bit will have the following meaning. DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. In PCMCIA Mode operation, Card 0 or 1 is selected using the copy field of the PC Card Socket and Copy configuration register.
- Bit 3 (HS3)** When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
- Bit 2 (HS2)** When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
- Bit 1 (HS1)** When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
- Bit 0 (HS0)** When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

**4.5.9. Status and Alternate Status Registers (Address 1F7[177] and 3F6[376]; Offsets 7 and Eh)**

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

- Bit 7 (BUSY)** The busy bit is set when the Industrial ATA product has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
- Bit 6 (RDY)** RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the Industrial ATA product is ready to accept a command.
- Bit 5 (DWF)** This bit, if set, indicates a write fault has occurred.
- Bit 4 (DSC)** This bit is set when the Industrial ATA product is ready.
- Bit 3 (DRQ)** The Data Request is set when the Industrial ATA product requires that information be transferred either to or from the host through the Data register.
- Bit 2 (CORR)** This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
- Bit 1 (IDX)** This bit is always set to 0.
- Bit 0 (ERR)** This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

**4.5.10. Device Control Register (Address—3F6[376]; Offset Eh)**

This register is used to control the card interrupt request and to issue an ATA soft reset to the card. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEh	0

- Bit 7** This bit is an X (Do not care).
- Bit 6** This bit is an X (Do not care).
- Bit 5** This bit is an X (Do not care).
- Bit 4** This bit is an X (Do not care).
- Bit 3** This bit is ignored by the card.

**Bit 2 (SW Rst)** This bit is set to 1 in order to force the card to perform an AT Disk controller Soft Reset operation. This does not change the PC Card Configuration Registers (4.3.2 to 4.3.5) as a hardware Reset does. The card remains in Reset until this bit is reset to '0'.

**Bit 1 (-IEn)** The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the card are disabled. This bit also controls the Int bit in the Configuration and Status Register. This bit is set to 0 at power on and Reset.

**Bit 0** This bit is ignored by the card.

#### 4.5.11. Card (Drive) Address Register (Address 3F7[377]; Offset Fh)

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

**Bit 7** This bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the Industrial ATA product. Following are some possible solutions to this problem for the PC Card implementation:

1. Locate the Industrial ATA product at a non-conflicting address (i.e., Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and an Industrial ATA product in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/O address 3F7/377 when an Industrial ATA product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the Industrial ATA product's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the Industrial ATA product or b) if provided use an additional Primary/Secondary configuration in the Industrial ATA product that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

**Bit 6 (-WTG)** This bit is 0 when a write operation is in progress, otherwise, it is 1.

**Bit 5 (-HS3)** This bit is the negation of bit 3 in the Drive/Head register.

**Bit 4 (-HS2)** This bit is the negation of bit 2 in the Drive/Head register.

**Bit 3 (-HS1)** This bit is the negation of bit 1 in the Drive/Head register.

**Bit 2 (-HS0)** This bit is the negation of bit 0 in the Drive/Head register.

**Bit 1 (-nDS1)** This bit is 0 when drive 1 is active and selected.

**Bit 0 (-nDS0)** This bit is 0 when the drive 0 is active and selected.

## 5. S.M.A.R.T. Functionality

Cactus Technologies® -603 series Compact Flash devices supports the following SMART commands, loaded into the Feature Register:

Value	Command
D0h	SMART read data
D1h	SMART read attribute thresholds

Value	Command
D2h	SMART enable/disable attribute autosave
D5h	SMART read log
D6h	SMART write log
D8h	SMART enable operations
D9h	SMART disable operations
DAh	SMART return status

The following sections describes these commands in detail.

## 5.1. SMART Enable Operations

This command enables access to the SMART features of the Cactus Technologies® -603 series Compact Flash devices. For this command to take effect, the following signature bytes must be loaded:

Cylinder Low - 4Fh

Cylinder High - C2h

The state of SMART (enabled/disabled) is preserved across power cycles.

## 5.2. SMART Disable Operations

This command disables access to the SMART features of the Cactus Technologies® -603 series Compact Flash devices. For this command to take effect, the following signature bytes must be loaded:

Cylinder Low - 4Fh

Cylinder High - C2h

The state of SMART (enabled/disabled) is preserved across power cycles.

## 5.3. SMART Enable/Disable Attribute Autosave

For this command to take effect, the following signature bytes must be loaded:

Sector Count - 00h or F1h

Cylinder Low - 4Fh

Cylinder High - C2h

This command is essentially a no-operation as the SMART attribute data is always available and kept current by the device..

## 5.4. SMART Read Data

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low - 4Fh

Cylinder High - C2h

This command returns one sector of SMART data. The format of the returned data is as follows:

Offset	Value	Description
0 – 1	0010h	SMART structure version
2 – 361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Offline data collection status (no offline data collection)
363	00h	Selftest execution status (selftest completed)
364 – 365	0000h	Total time to complete offline data collection
366	00h	----
367	00h	Offline data collection capability (none)
368 369	0003h	SMART capabilities
370	00h	Error logging capability (none)
371	00h	----
372	00h	Short selftest routine recommended polling time
373	00h	Extended selftest routine recommended polling time
374 – 385	00h	Reserved
386 – 387	0004h	SMART controller structure version
388 – 391		Firmware commit counter
392 – 395		Firmware wear level threshold
396	1	Global wear leveling active
397	1	Global bad block management active
398 – 401		Average flash block erase count
402 – 405		Number of flash blocks involved into wear leveling
406 – 409		Number of total ECC errors during firmware initialization
410 – 413		Number of correctable ECC errors during firmware initialization



Offset	Value	Description
414 – 510	00h	----
511		Data structure checksum

There are 12 attributes defined for the -603 series products. The following sections describe in detail what these attributes are.

### 5.4.1. Spare Block Count Attribute

This attribute gives information about the amount of available spare blocks. The data structure of this attribute is as follows:

Offset	Value	Description
0	196	Attribute ID
1 – 2	0003h	Flags – Pre-fail type, attribute is updated during normal operation
3		Attribute value – the value returned here is the percentage of spare blocks remaining summed over all flash chips
4	64h	Attribute value – worse value (fixed at 64h)
5 – 7		Sum of initial number of spare blocks over all flash chips
8 – 10		Sum of current number of spare blocks over all flash chips
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value is less than a preset threshold determined during at factory low level format process, the SMART Return Status will indicate a threshold exceeded condition.

### 5.4.2. Spare Block Count Worse Channel Attribute

This attribute gives information about the spare blocks in the flash channel with the lowest current number of spare blocks. The data structure of this attribute is as follows:

Offset	Value	Description
0	213	Attribute ID
1 – 2	0003h	Flags – Pre-fail type, attribute is updated during normal operation
3		Attribute value – this value is the worst percentage remaining on the channel
4	64h	Attribute value – worst value (fixed at 64h)
5 – 7		Initial number of spare blocks in the flash channel with the lowest current number of spare blocks

Offset	Value	Description
8 – 10		Current number of spare blocks in the flash channel with the lowest current number of spare blocks
11	00h	Reserved

### 5.4.3. Erase Count Attribute

This attribute gives information about the number of flash block erases performed. The data structure of this attribute is as follows:

Offset	Value	Description
0	229	Attribute ID
1 – 2	000Xh	Flags – Pre-fail or Advisory type, attribute is updated during normal operation
3		Attribute value – the value returned here is an estimation of the percentage of card life remaining based on the number of flash block erases that have occurred and the target number of erases per flash block.
4		Attribute value – worse value
5 – 10		Estimated total number of block erases
11	00h	Reserved

This attribute is used for the SMART Return Status command. If the attribute value is less than a preset threshold determined during at factory low level format process, the SMART Return Status will indicate a threshold exceeded condition.

The target number of erases is set during factory low level format time. The attribute flag – Pre-fail or Advisory, is also set at that time.

### 5.4.4. Total ECC Error Attribute

This attribute gives information about the total number of ECC errors on flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	203	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 8		Total number of ECC errors, correctable and uncorrectable
9 – 10		--

Offset	Value	Description
11	00h	Reserved

#### 5.4.5. Correctable ECC Error Attribute

This attribute gives information about the total number of correctable ECC errors on flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	204	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 8		Total number of correctable ECC errors
9 – 10		--
11	00h	Reserved

#### 5.4.6. UDMA CRC Error Attribute

This attribute gives information about the total number of UDMA CRC errors on flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	199	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 8		Total number of UDMA CRC errors
9 – 10		--
11	00h	Reserved

#### 5.4.7. Total Number of Reads Attribute

This attribute gives information about the total number of flash read commands. The data structure of this attribute is as follows:

Offset	Value	Description
0	232	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 10		Total number of flash read commands
11	00h	Reserved

### 5.4.8. Power On Count Attribute

This attribute gives information about the total number of power on cycles. The data structure of this attribute is as follows:

Offset	Value	Description
0	12	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 8		Total number of power on cycles
9 – 10		--
11	00h	Reserved

### 5.4.9. Total LBAs Written Attribute

This attribute gives information about the total amount of data written in units of 32MB. The data structure of this attribute is as follows:

Offset	Value	Description
0	241	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 10		Total number of LBAs written, divided by 65536
11	00h	Reserved

### 5.4.10. Total LBAs Read Attribute

This attribute gives information about the total amount of LBAs read in units of 32MB. The data structure of this attribute is as follows:

Offset	Value	Description
0	242	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 10		Total number of LBAs read, divided by 65536
11	00h	Reserved

### 5.4.11. Anchor Block Status Attribute

This attribute gives information about the total number time the Anchor block has been re-written, either by a repair operation or by firmware updates. The data structure of this attribute is as follows:

Offset	Value	Description
0	214	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3	64h	Attribute value – fixed at 100
4	64h	Attribute value – worse value (fixed at 64h)
5 – 8		Anchor block write count
9 – 10		--
11	00h	Reserved

### 5.4.12. TRIM Status Attribute

This attribute gives information about the percentage of card capacity that is in trimmed state. The range is from 0 to 99. The data structure of this attribute is as follows:

Offset	Value	Description
0	215	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3		Attribute value

Offset	Value	Description
4		Attribute value – worst value
5 – 10		--
11	00h	Reserved

### 5.4.13. Temperature Status Attribute

This attribute gives information about the current, min and max temperature. The attribute value is the current temperature and the worst value is the max temperature. The temperature data is retrieved every 4s. The data structure of this attribute is as follows:

Offset	Value	Description
0	194	Attribute ID
1 – 2	0002h	Flags – Advisory type, attribute is updated during normal operation
3		Attribute value
4		Attribute value – worst value
5		Current temperature
6		Min. temperature
7		Max. temperature
8 - 10		--
11	00h	Reserved

## 5.5. SMART Read Attribute Threshold

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low – 4Fh

Cylinder High – C2h

This command returns one sector of SMART attribute thresholds information. The format of the returned data is as follows:

Offset	Value	Description
0 – 1	0010h	SMART structure version
2 – 361		Attribute entries 1 to 30 (12 bytes each)
362 - 379	00h	Reserved

Offset	Value	Description
380 - 510	00h	--
511		Data structure checksum

The SMART attribute threshold entries are as follows:

### 5.5.1. Spare Block Count Attribute Threshold

Offset	Value	Description
0	196	Attribute ID
1		Spare block count attribute threshold defined during low level format
2 - 11	00h	Reserved

### 5.5.2. Spare Block Count Worst Channel Attribute Threshold

Offset	Value	Description
0	213	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.3. Erase Count Attribute Threshold

Offset	Value	Description
0	229	Attribute ID
1		Erase count attribute threshold defined during low level format
2 - 11	00h	Reserved

### 5.5.4. Total ECC Errors Attribute Threshold

Offset	Value	Description
0	203	Attribute ID
1	00h	None defined

Offset	Value	Description
2 - 11	00h	Reserved

### 5.5.5. Correctable ECC Errors Attribute Threshold

Offset	Value	Description
0	204	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.6. UDMA CRC Errors Attribute Threshold

Offset	Value	Description
0	199	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.7. Total Number of Reads Attribute Threshold

Offset	Value	Description
0	232	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.8. Power On Count Attribute Threshold

Offset	Value	Description
0	12	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved



### 5.5.9. Total LBA Written Attribute Threshold

Offset	Value	Description
0	241	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.10. Total LBA Read Attribute Threshold

Offset	Value	Description
0	242	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.11. Anchor Block Status Attribute Threshold

Offset	Value	Description
0	214	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.12. TRIM Status Attribute Threshold

Offset	Value	Description
0	215	Attribute ID
1	00h	None defined
2 - 11	00h	Reserved

### 5.5.13. Temperature Status Attribute Threshold

Offset	Value	Description
0	194	Attribute ID

Offset	Value	Description
1	00h	None defined
2 - 11	00h	Reserved

## 5.6. SMART Return Status

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low - 4Fh

Cylinder High - C2h

This command checks the health of the device. If either the Spare Block Count or the Erase Count attribute exceeded the factory preset threshold, signature values will be returned in the Cylinder Low/High registers as follows:

Cylinder Low - F4h

Cylinder High - 2Ch

If the thresholds are not exceeded, the Cylinder Low/High registers retain the initially loaded 4Fh/C2h values.

## 5.7. SMART Read Log

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low - 4Fh

Cylinder High - C2h

This command will return data of the SMART log. The following log addresses are defined:

Address	Description
0x00	Log Directory
0x80 – 0x9F	Host Vendor Specific Logs
0xA0	Reserved
0xA1	Reserved
0xA2	Reserved

The Log Directory at address 0x00 returns one sector of data that shows the number of sectors for Log addresses 1 to 255:

Offset	Value	Description
0 – 1	1	SMART Logging version
10 - 11	1	Number of sectors in the CFA Feature Set log

Offset	Value	Description
256 – 319	16	Number of sectors for Log addresses 0x80 to 0x9F
320 – 321	4	Number of sectors in the log at address 0xA0
322 – 323	1	Number of sectors in the log at address 0xA1
324 – 325	1	Number of sectors in the log at address 0xA2

All other bytes in the Log Directory are zero.

## 5.8. SMART Write Log

For this command to take effect, the following signature bytes must be loaded:

Cylinder Low - 4Fh

Cylinder High - C2h

This command is used to write data to the SMART logs. Only the Host Vendor Specific logs can be written.

## 6.CIS Description

This section describes the Card Information Structure (CIS) for the Cactus Technologies® CompactFlash Memory Cards.

**Table 6-25. Card Information Structure**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
000h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
002h	03h									Link is 3 bytes	Link to next Tuple
004h	D9h	Dev ID Type Dh = I/O			W 1	Speed 1h = 250ns				I/O Device, No WPS, 250ns	Device ID, WPS, Speed
006h	01h	1x			2K units				2 Kilobytes of Address Space	Device Size	
008h	FFh	List End Marker								End of Devices	End Marker
00Ah	1Ch	CISTPL_DEVICE_OC								Other Conditions Info Tuple	Tuple Code
00Ch	04h									Link is 4 bytes	Link to next tuple
00Eh	02h	Reserved 0						3 1	M 0	Conditions: Dual voltage card, 3V operation is allowed, and WAIT is not used	3 Volts Operation, Wait Function
010h	D9h	Dev ID Type Dh = I/O			W 1	Speed 01h=250nsec				I/O Device, No WPS, Speed is 250 nsec with Wait	Device ID, WPS, Speed
012h	01h	1x			2K units				2Kilobytes of Address Space	Device Size	
014h	FFh	List End Marker								End of Devices	End Marker
016h	18h	CISTPL_JEDEC_C								JEDEC ID Common Mem	Tuple Code
018h	02h									Link is 2 bytes	Link Length
01Ah	DFh	PCMCIA JEDEC Manufacturer's ID								First Byte of JEDEC ID for Cactus PC Card-ATA 12V	Byte 1, JEDEC ID of Device 1 (0-2K)
01Ch	01h	PCMCIA Code for PC Card-ATA No Vpp Required								Second Byte of JEDEC ID	Byte 2, JEDEC ID
01Eh	20h	CISTPL_MANFID								Manufacturer's ID Tuple	Tuple Code
020h	04h									Link is 4 bytes	Link Length
022h	00h	Low Byte of PCMCIA Manufacturer's Code								JEDEC Manufacturer's ID	Low Byte of PCMCIA Mfg ID
024h	00h	High Byte of PCMCIA Manufacturer's Code								Code of 0 because other byte is JEDEC 1 byte Manufacturer's ID	High Byte of PCMCIA Mfg ID
026h	00h	Low Byte of Product Code								Manufacturer specific info	Low Byte Product Code
028h	00h	High Byte of Product Code								Manufacturer specific info	High Byte Product Code

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
02Ah	21h	CISTPL_FUNCID								Function ID Tuple	Tuple Code	
02Ch	02h									Link length is 2 bytes	Link to next tuple	
02Eh	04h	Function Type Code								Disk Function	Function Code	
030h	01h	R	R	R	R	R	R	R	P	Attempt installation at Post P: Install at POST R: Reserved (0)		
		0	0	0	0	0	0	0	1			
032h	22h	CISTPL_FUNCCE								Function Extension Tuple	Tuple Code	
034h	02h									Link length is 2 bytes	Link to next tuple	
036h	01h	Disk Function Extension Tuple Type								Extension tuple describes the Interface Protocol	Extension Tuple Type for Disk	
038h	01h	Interface Type Code								PC Card-ATA Interface	Extension Info	
03Ah	22h	CISTPL_FUNCCE								Function Extension tuple	Tuple Code	
03Ch	03h									This tuple has 3 info bytes	Link Length	
03Eh	02h	Disk Function Extension Tuple Type								Basic PCMCIA-ATA Extension tuple	Extension Tuple Type for Disk	
040h	04h	R	R	R	R	U	S	V		No Vpp, Silicon Drive with no Unique Manufacturer/Serial Number combined string V=0:No Vpp Required S:Silicon, else Rotating U:ID Drive Mfg/SN not Unique	Basic ATA Option Parameters	
		0	0	0	0	0	1	0				
042h	07h	R	I	E	N	P3	P2	P1	P0	All power down modes and power commands are not needed to minimize power. P0:Sleep Mode Supported P1:Standby Mode Supported P2:Idle Mode Supported P3:No Drive Auto Power Control N:Some Config includes 3X7 E:Index Bit not Emulated I:Twin -IOis16 unspecified	Extended ATA Option Parameters	
		0	0	0	0	0	1	1	1			
044h	1Ah	CISTPL_CONF								Configuration Tuple	Tuple Code	
046h	05h									Link Length is 5 bytes	Link to next tuple	
048h	01h	RF	RM	RAS							Size of Reserved Field is 0 bytes, Size of Register Mask is 1 Byte, Size of Config Base Address is 2 bytes RFS:Bytes in Reserved Field RMS:Bytes in Reg Mask-1 RAS:Bytes in Base Addr-1	Size of fields byte (TPCC_SZ)
		S	S	01								
		00	00									
04Ah	07h	TPCC_LAST								Entry with Config Index of 07h is final entry in table	Last entry of configuration table	
04Ch	00h	TPCC_RADR (lsb)								Configuration Registers are	Location of	
04Eh	02h	TPCC_RADR (msb)								located at 200h in Reg Space.	Config Registers	
050h	07h	R	R	R	R	S	P	C	I	First 3 Configuration Registers are present I:Configuration Index C:Configuration and Status P:Pin Replacement S:Socket and Copy R:Reserved for future use	TPCC_RMSK	
		0	0	0	0	0	1	1	1			
052h	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code	
054h	0Bh									Link to next tuple is 11 bytes. Also limits size of this tuple to 13 bytes.	Link to next tuple	

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
056h	C0h	I 1	D 1	Configuration Index 0						<b>Memory Mapped I/O Configuration</b> Configuration Index for this entry is 0. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows	TPCE_INDx	
058h	C0h	W 1	R 1	P 0	B 0	Interface Type 0					Memory Only Interface(0), Bvd's and wProt not used, Ready/-Busy and Wait for memory cycles active. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF
05Ah	A1h	M 1	MS 1	IR 0	IO 0	T 0	P 1	Vcc only Power; No Timing, I/O, or IRQ; 2 Byte Mem Space Length; Misc Entry Present P:Power info type T:Timing info not present IO:I/O space not used IR:Interrupt not used MS:Mem space info type M:Misc info byte(s) present			TPCE_FS	
05Ch	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal Voltage Follows NV:Nominal Voltage info present LV:Minimum Voltage info present HB:Maximum Voltage info present SI:No Static Current info AI:No Average Current info PI:Peak Current info present DI:No Power Down Current info	Power Parameters for Vcc	
05Eh	55h	X 0	Mantissa Ah = 5.0			Exponent 5h = 1V			Vcc Nominal is 5 Volts			Vcc Nominal Value
060h	4Dh	X 0	Mantissa 9h = 4.5			Exponent 5h = 1V			Vcc Minimum is 4.5 Volts			Vcc Minimum Value
062h	5Dh	X 0	Mantissa Bh = 5.5			Exponent 5h = 1V			Vcc Maximum is 5.5 Volts			Vcc Maximum Value
064h	75h	X 0	Mantissa Eh = 8.0			Exponent 5h = 10			Peak Current is 80 mA			Peak Current
066h	08h	Length in 256 bytes pages (lsb)								Length of Mem Space is 2 KB	TPCE_MS Length LSB	
068h	00h	Length in 256 bytes pages (msb)								Start at 0 on card	TPCE_MS Length MSB	
06Ah	20h	X 0	R 0	P 1	RO 0	A 0	T 0			Power Down, and Twin Card. T: Twin Cards not supported A: Audio Not Supported RO: Read/Write Mode P: Power Down Supported R: Reserved X: No more Misc Fields Bytes	TPCE_MI	
06Ch	1Bh	CISTPL_CE								Configuration Entry tuple	Tuple code	

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
06Eh	06h	CISTPL_LINK								Link to next tuple is 6 bytes	link to next tuple	
070h	00h	ID Configuration Index								Memory mapped configuration, index=0	TCPCE_INDX	
072h	01h	M	MS	IR	IO	T	P			P:Power info type No Vpp	TPCE_FS	
		0	0	0	0	0	1					
074h	21h	R	DI	PI	AI	SI	H	LV	NV	PI:Peak Current Info NV:Nominal Operation Supply Voltage Info	TPCE_PD	
		0	0	1	0	0	0	0	1			
076h	B5h	X	Mantissa 6h = 3.0			Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V Extension Byte Present		Nominal Operation Supply Voltage	
		1										
078h	1Eh	X	1Eh								+ .30	Nominal Operation Supply Voltage Extension Byte
		0										
07Ah	4Dh	X	Mantissa 9h = 4.5			Exponent 5h = 10			Max Average Current over 10 msec is 45mA		Max Average Current	
		0										
07Ch	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code	
07Eh	0Dh									Link to next tuple is 13 bytes. Also limits size of this tuple to 15 bytes.	Link to next tuple	
080h	C1h	I	D	Configuration Index 1						<b>I/O Mapped Contiguous 16 registers configuration</b> Configuration Index for this entry is 1. Interface Byte follows this byte. Default Configuration, so is not dependent on previous Default Configuration. D:Default Configuration I:Interface Byte Follows		TPCE_INDX
		1	1									
082h	41h	W	R	P	B	Interface Type 1				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Used for Memory Cycles	TPCE_IF	
		0	1	0	0							
084h	99h	M	MS	IR	IO	T 0				M: misc info present MS: no memory space info IR: Interrupt used IO: I/O space used T: No Timing info	Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present P:Power info type T:Timing info present IO:I/O port info present IR:Interrupt info present MS:Mem space info type M:Misc info byte(s) present	
		1	0	1	1							
086h	27h	R	DI	PI	AI	SI	HV	L	N	Nominal Voltage Follows NV:Nominal Voltage info LV:Minimum Voltage info HB:Maximum Voltage info SI:No Static Current info AI:No Average Current info PI:Peak Current info DI:No Power Down Current info	Power Parameters for Vcc	
		0	0	1	0	0	1	1	1			
088h	55h	X	Mantissa Ah = 5.0			Exponent 5h = 1V			Vcc Nominal is 5Volts		Vcc Nominal Value	
		0										
08Ah	4Dh	X	Mantissa 9h = 4.5			Exponent 5h = 1V			Vcc Minimum is 4.5 Volts		Vcc Minimum Value	
		0										

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
08Ch	5Dh	X 0		Mantissa Bh = 5.5			Exponent 5h = 1V			Vcc Maximum is 5.5Volts	Vcc Maximum Value	
08Eh	75h	X 0		Mantissa Eh = 8.0			Exponent 5h = 10			Max Average Current over 10 msec is 80 mA	Max Average Current	
090h	64h	R 0	S 1	E 1	IO AddeLines 4					Supports both 8 and 16 bit I/O hosts. 4 Address lines and no range so 16 registers and host must do all selection decoding. IOAddrLines:4 addresses decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO	
092h	F0h	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active in Card Control and Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Present V:No Vendor Unique IRQ B:No Bus Error IRQ I:No IO Check IRQ N:No Non-Maskable IRQ	TPCE_IR	
094h	FFh	IRQ[7:0]								Interrupts may be assigned to any host IRQs		
096h	FFh	IRQ[15:8]										
098h	20h	X 0	R 1	P 0	R O 0	A 0	T 0				X=0; no more misc field P=1; pwr down supported R/O=0; rd/wr media A=0; audio not supported T=0; twin card not supported	TPCE_MI
09Ah	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code	
09Ch	06h									Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.	Link to next tuple	
09Eh	01h	I 0	D 0	Configuration Index 1						I/O mapped contiguous 16 3.3V configuration	TPCE_INDX	
0A0h	01h	M 0	MS 0	IR 0	IO 0	T 0	P 1				P:Power info type No Vpp	TPCE_FS
0A2h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	N V 1	PI:Peak Current Info NV:Nominal Operation Supply Voltage Info	Power Parameters for Vcc	
0A4h	B5h	X 1	Mantissa 6h = 3.0				Exponent 5h = 1				Nominal Operation Supply Voltage = 3.0V Extension Byte Present	Nominal Operation Supply Voltage
0A6h	1Eh	X 0	1Eh								+30	Nominal Operation Supply Voltage Extension Byte
0A8h	4Dh	X 0	Mantissa 9h = 4.5				Exponent 5h = 10				Max Average Current over 10 msec is 45 mA	Max Average Current
0AAh	1Bh	CISTPL_CE								Configuration Entry Tuple	Tuple Code	



Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
0ACh	12h									Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.	Link to next tuple	
0AEh	C2h	I	D	Configuration Index							<b>AT Fixed Disk Primary I/O Address Configuration</b> Configuration Index for this entry is 2. Interface Byte follows this byte. Default Configuration	TPCE_INDX
0B0h	41h	W	R	P	B	Interface Type				I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Not Used for Memory Cycles	TPCE_IF	
0B2h	99h	M	MS	IR	IO	T	P				Vcc Only Power Description; No Timing; I/O and IRQ present; No Mem Space; Misc Entry present P:Power info type T:No Timing info present IO:I/O port info present IR:Interrupt info present MS:No Mem space info M:Misc info byte(s) present	TPCE_FS
0B4h	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal Voltage Follows NV:Nominal Voltage LV:Minimum Voltage HB:Maximum Voltage SI:No Static Current info AI:No Average Current info PI:Peak Current DI:No Power Down Current info	Power Parameters for Vcc	
0B6h	55h	X	Mantissa Ah = 5.0			Exponent 5h = 1V			Vcc Nominal is 5Volts			Vcc Nominal Value
0B8h	4Dh	X	Mantissa 9h = 4.5			Exponent 5h = 1V			Vcc Minimal is 4.5Volts			Vcc Minimum Value
0BAh	5Dh	X	Mantissa Bh = 5.5			Exponent 5h = 1V			Vcc Maximum is 5.5Volts			Vcc Maximum Value
0BCh	75h	X	Mantissa Eh = 8.0			Exponent 5h = 10			Max Average Current over 10 msec is 80 mA			Max Average Current
0BEh	EAh	R	S	E	IO AddeLines Ah = 10				Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (1F0-1F7, 3F6-3F7) on A9 through A0 for I/O cycles. IO AddrLines10 lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows			TPCE_IO

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function			
0C0h	61h	LS 1	AS 2	N Ranges - 1 1							Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description		
0C2h	F0h	1st I/O Base Address (lsb)			First I/O Range base is									
0C4h	01h	1st I/O Base Address (msb)			1F0h									
0C6h	07h	1st I/O Range Length - 1			8 bytes total ==> 1F0-1F7h				I/O Length - 1					
0C8h	F6h	2nd I/O Base Address (lsb)			2nd I/O Range base is									
0CAh	03h	2nd I/O Base Address (msb)			3F6h									
0CCh	01h	2nd I/O Range Length - 1			2 bytes total ==> 3F6-3F7h				I/O Length - 1					
0CEh	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14			IRQ Sharing Logic Active in Card Control and Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs not Supported M=0 so bits 3-0 are single level, binary encoded				TPCE_IR	
0D0h	20h	X 0	R 0	P 1	RO 0	A 0	T 0			Power-Down, and Twin Card. T:Twin Cards not supported A:Audio Not Supported RO:Read/Write Mode P:Power Down Supported R:Reserved X:No More Misc Fields Bytes				TPCE_MI
0D2h	1Bh	CISTPL_CE			Configuration Entry Tuple				Tuple Code					
0D4h	06h				Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.				Link to next tuple					
0D6h	02h	I 0	D 0	Configuration Index 2			AT Fixed Disk Primary I/O 3.3V configuration				TPCE_INDX			
0D8h	01h	M 0	MS 0	IR 0	IO 0	T 0	P 1			P:Power info type				TPCE_FS

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
0DAh	21h	R	DI	PI	AI	SI	HV	LV	NV	PI:Peak Current INfo NV:Nominal Operation Supply Voltage Info	Power Parameters for Vcc	
		0	0	1	0	0	0	0	1			
0DCh	B5h	X	Mantissa 6h = 3.0			Exponent 5h = 1			Nominal Operation Supply Voltage = 3.0V Extension Byte Present		Nominal Operation Supply Voltage	
0DEh	1Eh	X	1Eh			+30			Nominal Operation Supply Voltage Extension Byte			
0E0h	4Dh	X	Mantissa 9h = 4.5			Exponent 5h = 10			Max Average Current over 10 msec is 45mA		Max Average Current	
0E2h	1Bh	CISTPL_CE			Configuration Entry Tuple			Tuple Code				
0E4h	12h	Link to next tuple is 18 bytes. Also limits size of this tuple to 20 bytes.			Link to next tuple							
0E6h	C3h	I	D	Configuration Index 3			<b>AT Fixed Disk Secondary I/O Address Configuration</b> Configuration Index for this entry is 3. Interface Byte follows this byte. Default Configuration			TPCE_INDx		
		1	1									
0E8h	41h	W	R	P	B	Interface Type 1			I/O Interface(1), Bvd's and wProt not used; Ready/-Busy active but Wait not used for memory cycles. B:Battery Volt Detects Not Used P:Write Protect Not Used R:Ready/-Busy Used W:Wait Not Used for Memory Cycles		TPCE_IF	
		0	1	0	0							
0EAh	99h	M	MS	IR	IO	T	P			Vcc Only Power Descriptors; No Timing; I/O and IRQ present; No Mem Space; Misc Entry Present. P:Power info type T:No Timing info present IO:I/O port info present IR:Interrupt info present MS:No Mem space info type M:Misc info byte(s) present		TPCE_FS
		1	0	1	1	0	1					
0ECh	27h	R	DI	PI	AI	SI	HV	LV	NV	Nominal Voltage Follows NV:Nominal Voltage info LV:Minimum Voltage info HV:Maximum Voltage info SI:No Static Current info AI:No Average Current info PI:Peak Current DI:No Power Down Current info	Power Parameters for Vcc	
		0	0	1	0	0	1	1	1			
0EEh	55h	X	Mantissa Ah = 5.0			Exponent 5h = 1V			Vcc Nominal is 5Volts		Vcc Nominal Value	
		0										
0F0h	4Dh	X	Mantissa 9h = 4.5			Exponent 5h = 1V			Vcc Minimum is 4.5Volts		Vcc Minimum Value	
		0										
0F2h	5Dh	X	Mantissa Bh = 5.5			Exponent 5h = 1V			Vcc Maximum is 5.5Volts		Vcc Maximum Value	
		0										
0F4h	75h	X	Mantissa Eh = 1.0			Exponent 5h = 10			Max Average Current over 10 msec is 80 mA		Max Average Current	
		0										

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
0F6h	EAh	R 1	S 1	E 1	IO AddeLines Ah = 10					Supports both 8 and 16 bit I/O hosts. 10 Address lines with range so card will respond only to indicated (170-177, 376-377) on A9 through A0 for I/O cycles. IO AddrLines10 lines decoded E:Eight bit only hosts supported S:Sixteen bit hosts supported R:Range Follows	TPCE_IO
0F8h	61h	LS 1		AS 2		N Ranges-1 1				Number of Ranges is 2; Size of each address is 2 bytes; Size of each length is 1 byte. AS:Size of Addresses 0:No Address Present 1:1Byte (8 bit) Addresses 2:2Byte (16 bit) Addresses 3:4Byte (32 bit) Addresses LS:Size of length 0:No Lengths Present 1:1Byte (8 bit) Lengths 2:2Byte (16 bit) Lengths 3:4Byte (32 bit) Lengths	I/O Range Format Description
0FAh	70h	1st I/O Base Address (lsb)					First I/O Range base is				
0FCh	01h	1st I/O Base Address (msb)					170h				
0FEh	07h	1st I/O Range Length - 1					8 bytes total ==> 170-177h				I/O Length - 1
100h	76h	2nd I/O Base Address (lsb)					2nd I/O Range base is				
102h	03h	2nd I/O Base Address (msb)					376h				
104h	01h	2nd I/O Range Length - 1					2 bytes total ==> 376-377h				I/O Length - 1
106h	EEh	S 1	P 1	L 1	M 0	Recommend IRQ Level Eh = 14				IRQ Sharing Logic Active in Card Control and Status Register, Pulse and Level Mode Interrupts supported, Recommended IRQ's any of 0 through 15(F) S:Share Logic Active P:Pulse Mode IRQ Supported L:Level Mode IRQ Supported M:Bit Mask of IRQs Not Present M=0 so bits 3-0 are single level, binary encoded	TPCE_IR
108h	20h	X 0	R 0	P 1	RO 0	A 0	T 0			Power-Down, and Twin Card. T:Twin Cards not supported A:Audio Not Supported RO:Read/Write Mode P:Power Down Supported R:Reserved X:No More Misc Fields Bytes	TPCE_MI
10Ah	1Bh	CISTPL_CE					Configuration Entry Tuple				Tuple Code
10Ch	06h						Link to next tuple is 6 bytes. Also limits size of this tuple to 8 bytes.				Link to next tuple
10Eh	03h	I 0	D 0	Configuration Index 3						AT Fixed Disk Secondary I/O 3.3V configuration	TPCE_INDX
110h	01h	M 0	MS 0	IR 0	IO 0	T 0	P 1			P:Power info type	TPCE_FS

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
112h	21h	R	DI	PI	AI	SI	HV	LV	NV	PI:Peak Current NV:Nominal Operation Supply Voltage	Power Parameters for Vcc	
		0	0	1	0	0	0	0	1			
114h	B5h	X	Mantissa 6h = 3.0			Exponent 5h = 1					Nominal Operation Supply Voltage = 3.0V Extension Byte Present	Nominal Operation Supply Voltage
116h	1Eh	X	1Eh			+.30					Nominal Operation Supply Voltage Extension Byte	
118h	4Dh	X	Mantissa 9h = 4.5			Exponent 5h = 10					Max Average Current over 10 msec is 45mA	Max Average Current
11Ah	014h		CISTPL_NO_LINK								Prevent Scan of Common Memory	Tuple Code
11Ch	000h		CISTPL_LINK								Link Length is 0 Bytes	Link to next tuple
11Eh	015h		CISTPL_VERS_1								Level 1 version/product info	Tuple Code
120h	015h		CISTPL_LINK								Link Length is 21h bytes	Link to next tuple
122h	004h		TPPLV1_MAJOR								PCMCIA 2.0/JEIDA 4.1	Major Version
124h	001h		TPPLV1_MINOR								PCMCIA 2.0/JEIDA 4.1	Minor Version
126h	...										Cactus	Info String 1
146h	...										Model	Info String 2
15Ch	0FFh		CISTPL_END								End of CISTPL_VERS_1	End Marker
15Eh	0FFh		CISTPL_END								End of CIS	Tuple code

# Appendix A. Ordering Information

Model KCXYZ-603

Where: X is card capacity

- 128M ----- 128MB
- 256M ----- 256MB
- 512MB ----- 512MB
- 1G ----- 1GB
- 2G ----- 2GB
- 4G ----- 4GB
- 8G ----- 8GB
- 16G ----- 16GB
- 32G ----- 32GB
- 64G ----- 64GB

Where Y is card configuration

- R ----- Removable card
- F ----- Fixed card

If your systems cannot accept removable CF card (R), then please order Fixed CF card (F).

Where Z is temperature

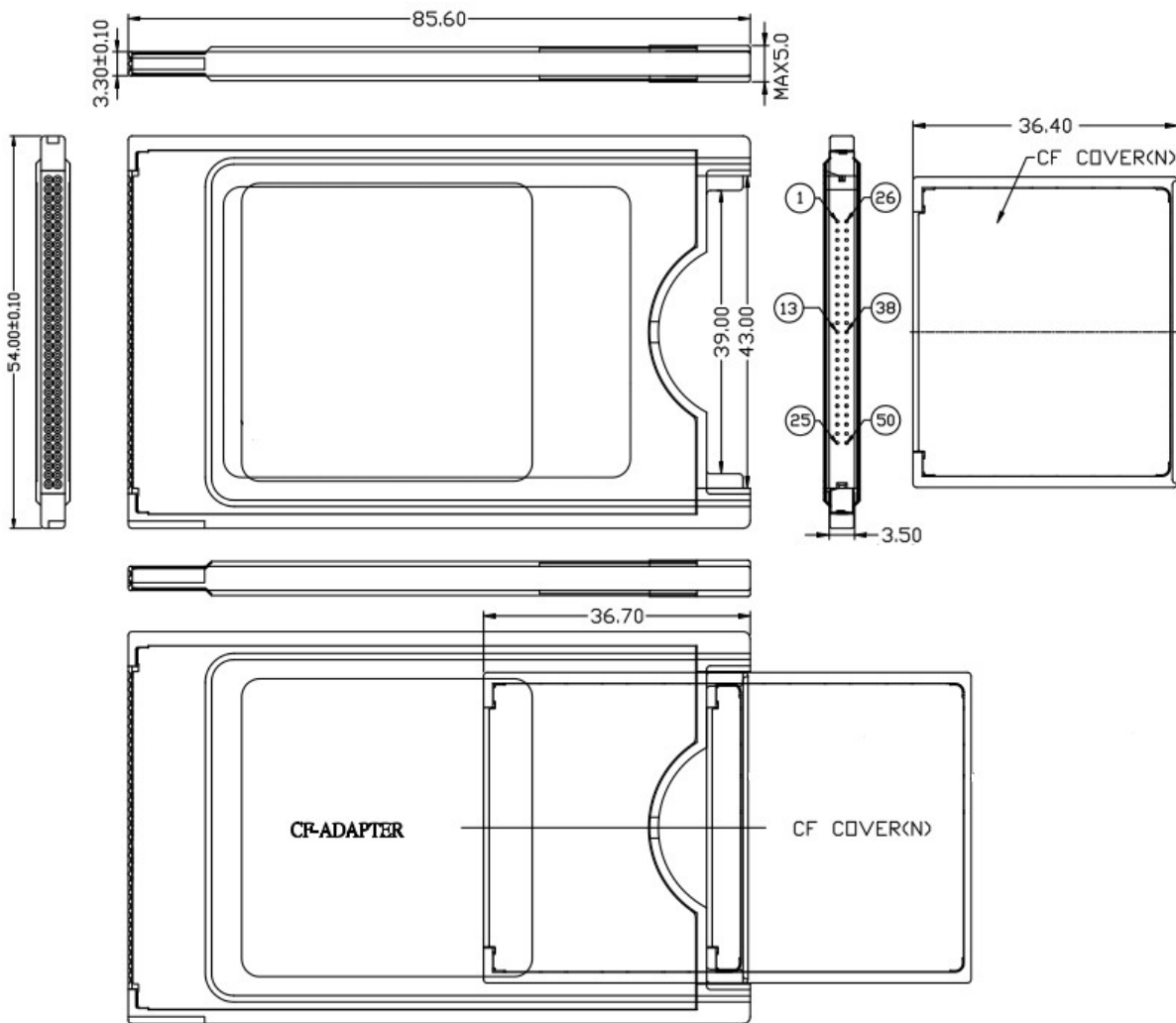
- Blank ----- Standard temperature (0° C to +70° C)
- I ----- Extended temperature (-40° C to +85° C)

Example:

- (1) 1GB CF Removable Extended Temp ----- KC1GRI-603
- (2) 2GB CF Fixed ----- KC2GF-603

## Appendix B.CF To PC Card Adapter Information

For customers who would like to use the Cactus Technologies® CompactFlash cards in their existing PC Card sockets, we offer a CF to PC Card adapter. The physical dimensions of this adapter are as shown below:



To order this adapter, please use the following product code:

KADPT-CF02

## **Appendix C. Technical Support Services**

Email: [tech@cactus-tech.com](mailto:tech@cactus-tech.com)



## **Appendix D. Cactus Technologies® Worldwide Sales Offices**

Email: [sales@cactus-tech.com](mailto:sales@cactus-tech.com)

Email: [americas@cactus-tech.com](mailto:americas@cactus-tech.com)

# Appendix E.Limited Warranty

## I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited

## II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® Industrial Grade CompactFlash Card. In satisfaction of its obligations hereunder, Cactus Technologies®, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

Cactus Technologies® products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

## III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing or replacing the defective product, if the following conditions are met:

- A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.
- B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.
- C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

Cactus Technologies® reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

Cactus Technologies® may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, Cactus Technologies® also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product's specifications.

#### **IV. RECEIVING WARRANTY SERVICE**

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number with instructions to ship the product back to us for service.