Cactus®
Technologies

300 Series Industrial Grade DiskOnModule (DOM)

Product Manual

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01 Introduction to Cactus Technologies 300 Series Industrial Grade DOM Products

Features

- Solid state design with no moving parts
- Plugs into industry standard IDE 40/44 pin sockets.
- Supports ATA PIO Modes 0-4
- Supports MultiWord DMA Modes 0-2
- Supports UDMA Modes 0-4
- High reliability, MTBF > 4,000,000 hrs.
- Enhanced error correction, < 1 error in 10^{14} bits read
- Comes in Vertical, Horizontal Left and Horizontal Right configurations
- Dual voltage support: 3.3V/5.0V

Overview

The Cactus Technologies DiskOnModule (DOM) is a low capacity solid-state flash memory product that complies with the ANSI ATA standard and is electrically compatible with an IDE disk drive. Cactus DOMs provide up to 8GB of formatted storage capacity and is designed to plug in directly to IDE connectors on an industrial PC motherboard. Cactus DOMs are designed to be used in applications which requires a low capacity solid state disk that is IDE compatible.

The Cactus Technologies Industrial Grade DOM products use high quality flash memory from well known vendors, such as Samsung Corporation. In addition, it include an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller's firmware is upgradeable, thus allowing feature enhancements and firmware updates in the field.

1.1. Supported Standards

Cactus Technologies DOM is fully electrically compatible with the following specification:

- ATA 5 Specification published by ANSI: X3.221 AT Attachment Interface for Disk Drives

1.2. Product Features

Cactus Technologies Industrial DOM contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies Industrial DOM appears as a standard ATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the ATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies Industrial DOM products today will continue to work with future Cactus Technologies Industrial DOMs built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies Industrial DOM contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies Industrial DOMs is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies Industrial DOMs unparalleled reliability.

1.2.3. Intelligent Power Management

Cactus Technologies Industrial DOM employs sophisticated power management algorithms to conserve power. Upon completion of a command, the drive will automatically enter sleep mode if no further commands are received. In most situations, the drive will be in sleep mode except when the host is accessing it, thus conserving power.

When the drive is in sleep mode, any command issued to the drive will cause it to exit sleep and respond.

02 Power Supply Requirements

Cactus Technologies Industrial DOM is a dual voltage product, which means it will operate at a voltage range of 3.30 volts ±10% or 5.00 volts ± 10%.Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Industrial DOM
Temperature	**Operating:**	0° C to +70° C (Standard) -45° C to +90° C (Extended)
Humidity	**Operating & Non-Operating:**	8% to 95%, non-condensing
Acoustic Noise		0 dB
Vibration	**Operating & Non-Operating:**	20 G MIL-STD-883G Method 2005.2 condition A
Shock	**Operating & Non-Operating:**	3,000 G MIL-STD-883G Method 2002.3 condition C
Altitude (relative to sea level)	**Operating & Non-Operating:**	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Industrial DOM
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		3.3V ±10% or 5.0V ±10%
(Maximum Average Value) See Notes.	**Sleep:** **Reading:** **Writing:**	500 µA 220 mA 180 mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance numbers are typical values assuming the card controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Start Up Times	**Reset to ready:**	35 msec typical
Read Transfer Rate		up to 35.0 Mbytes/sec*
Write Transfer Rate		up to 20.0 Mbytes/sec *
Controller Overhead	**Command to DRQ**	2 msec maximum

2.4. System Reliability

Table 2-4. Reliability

MTBF (@ 25°C)	>4,000,000 hours
Data Reliability	<1 non-recoverable error in 10^{14} bits READ
Endurance:	>2,000,000 erase/program cycles

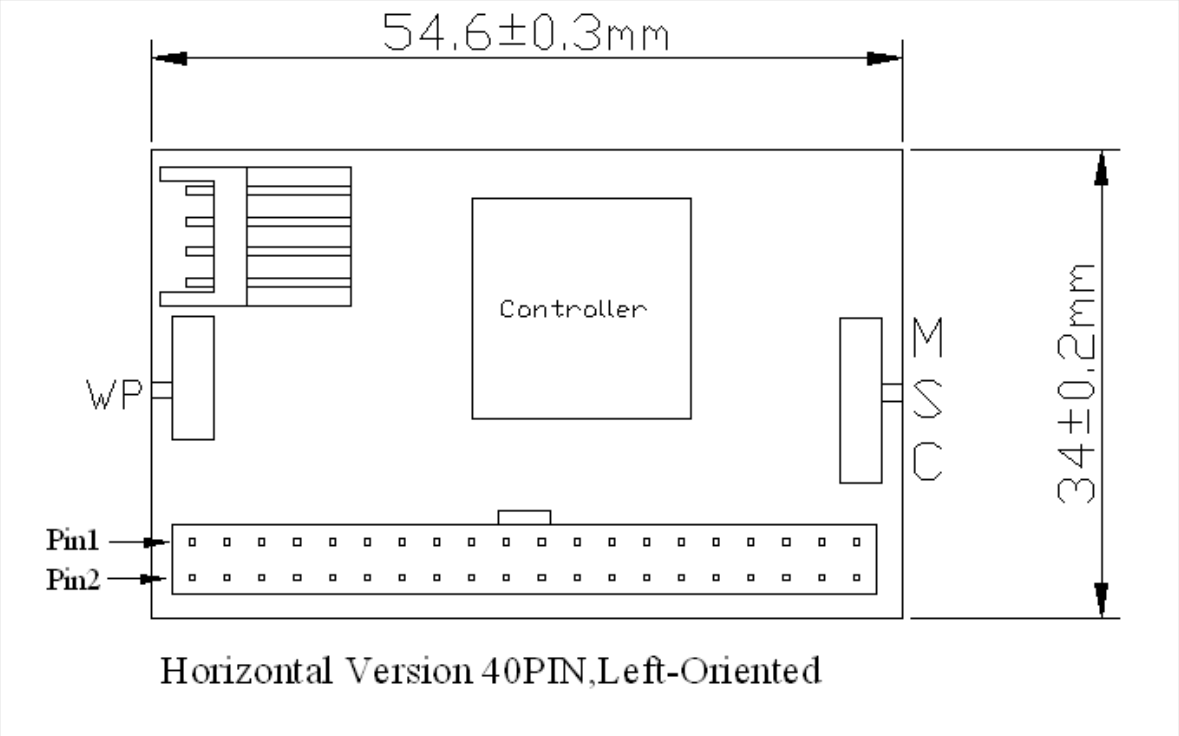
2.5. Physical Specifications

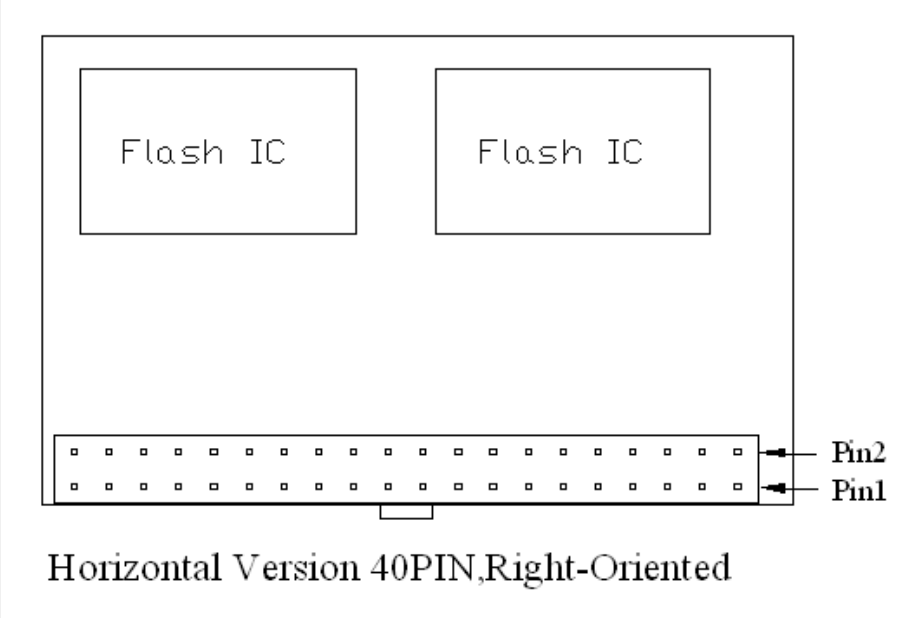
The following sections provide the physical specifications for Cactus Technologies Industrial DOM products.

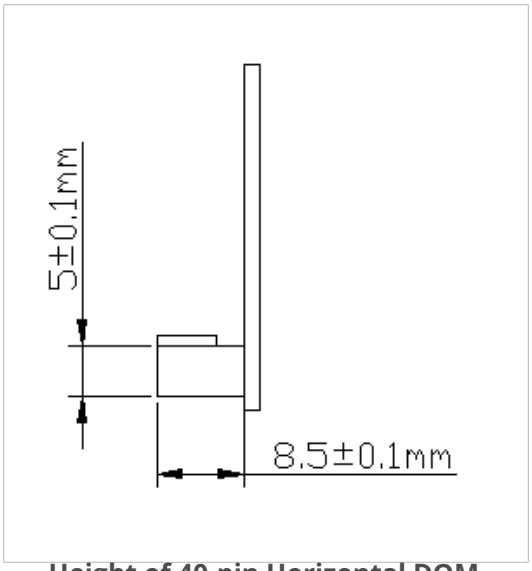
2.5.1. DOM Physical Specifications

Refer to Figure 2-1 for Cactus 40-pin DOM physical specifications and dimensions and Figure 2-2 for Cactus 44-pin DOM physical specifications.

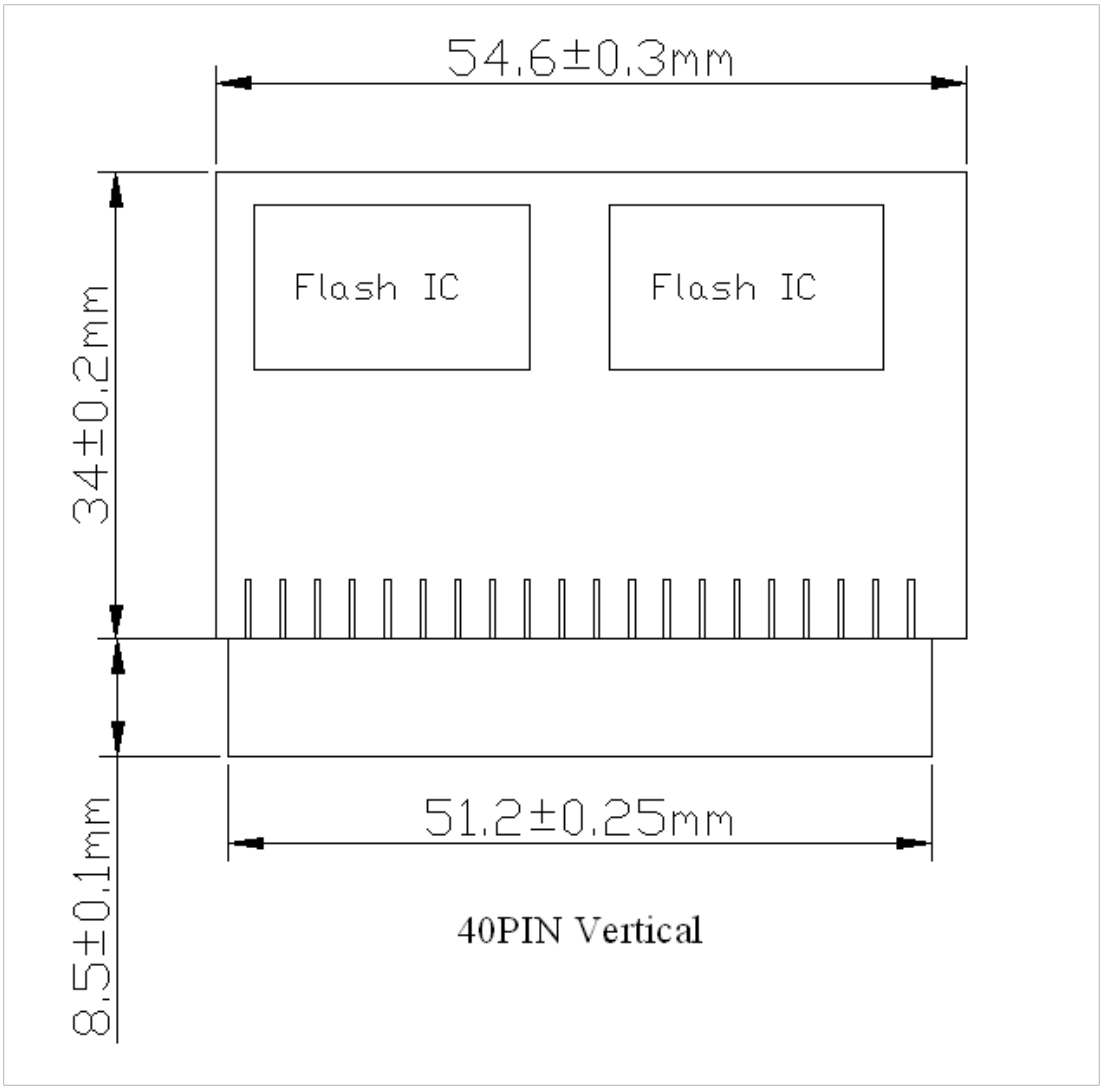
Figure 2-1. 40-pin DOM physical specifications

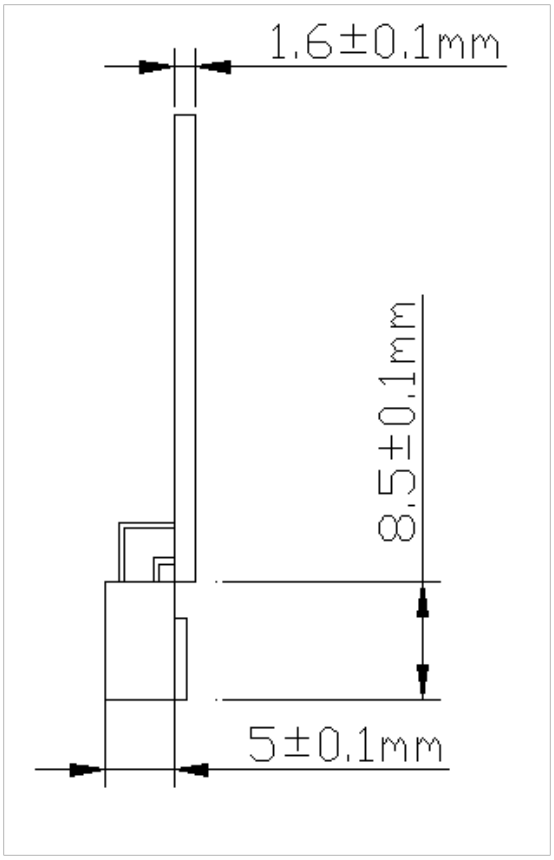


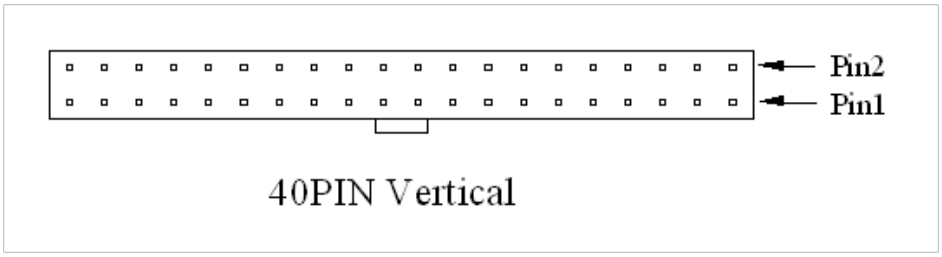




Height of 40-pin Horizontal DOM

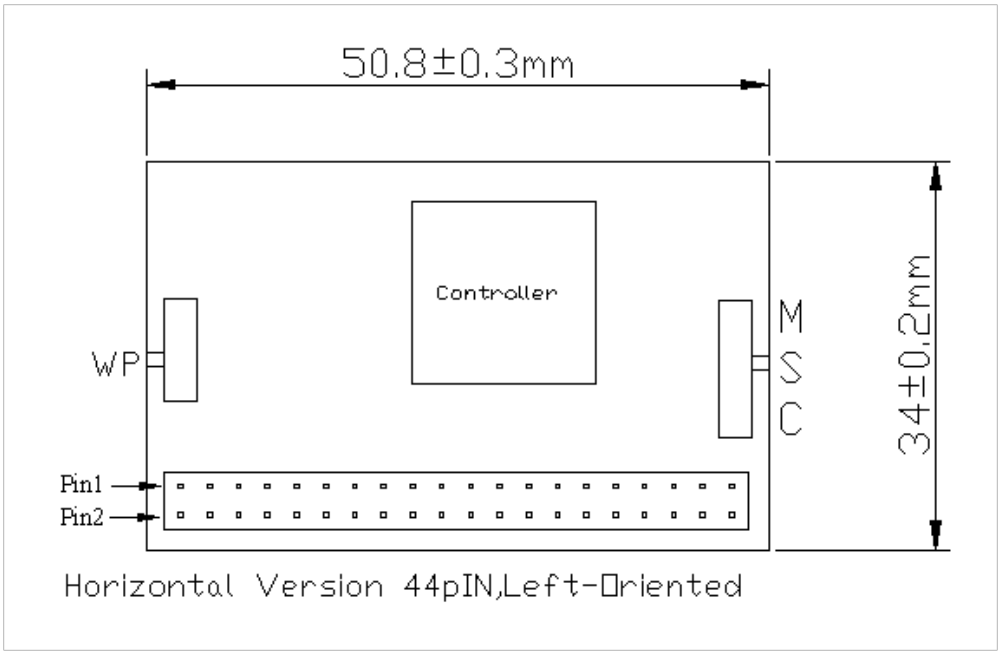


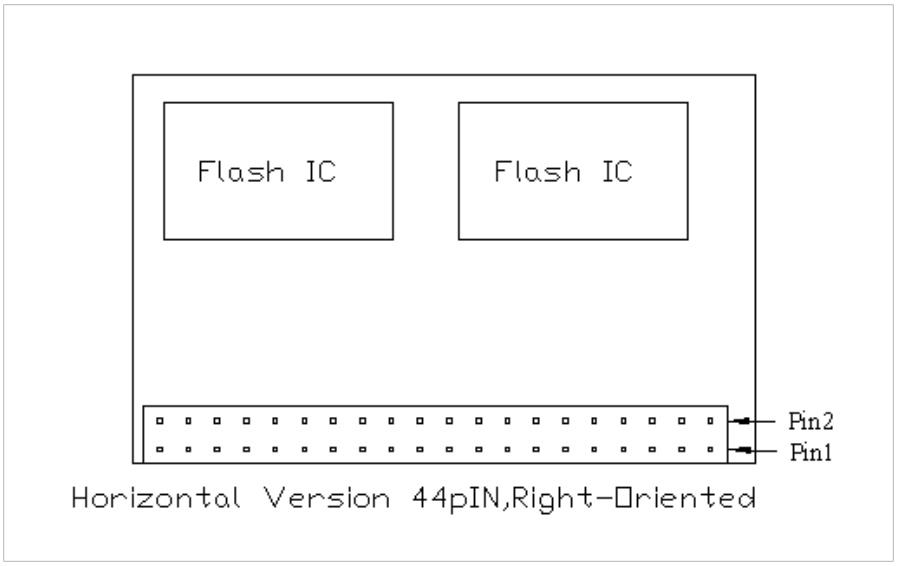


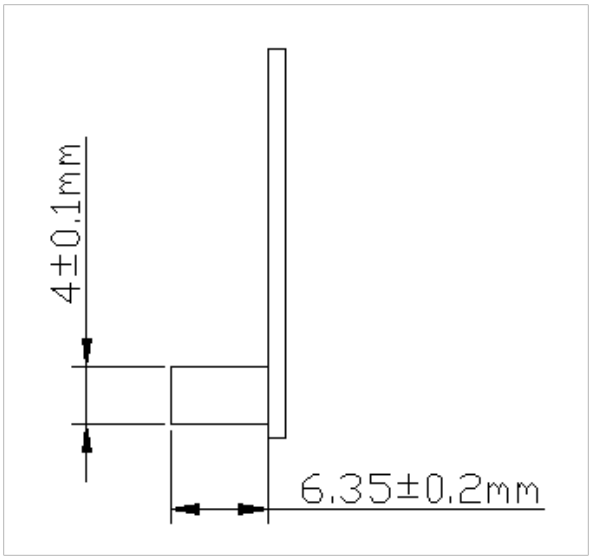


40PIN Vertical

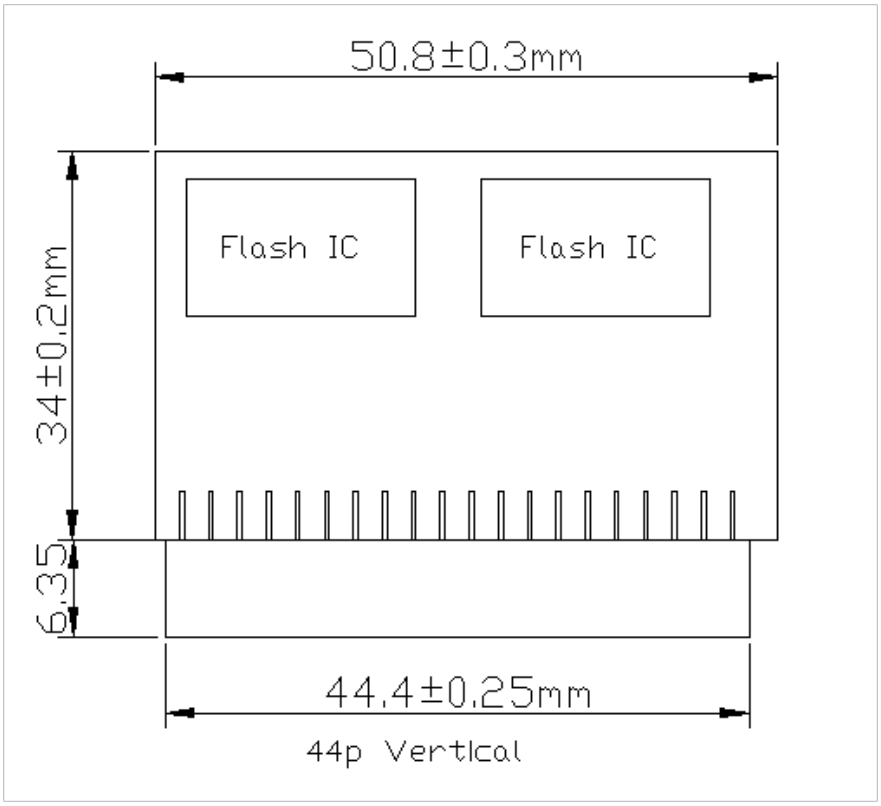
Figure 2-2. 44-pin DOM physical specifications

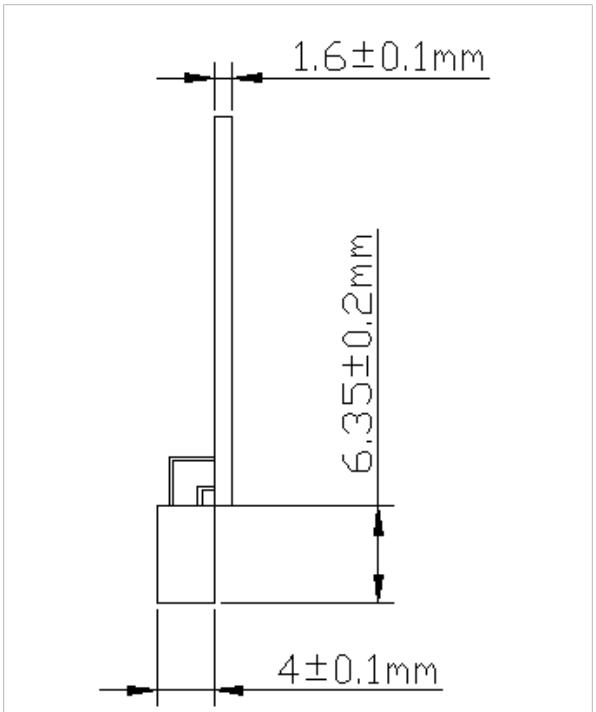






Height of 44-pin DOM




1.6±0.1mm
6.35±0.2mm
4±0.1mm

2.6. Capacity Specifications

The following sections provide capacity specifications for Cactus Technologies DOM products.

2.6.1. DOM Capacity Specifications

Table 2-5 shows the specific capacity for the various models and the default number of heads, sectors/track and cylinders.

Table 2-5. Model Capacities

Capacity	Capacity (formatted)	Sectors/ Drive (Max LBA+1)	No. of Heads	No. of Sectors/ Track	No. of Cylinders
128MB	**129,761,280 bytes**	253,440	8	32	990
256MB	**259,522,560 bytes**	506,880	16	32	990
512MB	**521,256,960 bytes**	1,018,080	16	63	1,010
1GB	**1,047,674,880 bytes**	2,046,240	16	63	2,030
2GB	**2,097,930,240 bytes**	4,097,520	16	63	4,065
4GB	**4,224,245,760 bytes**	8,250,480	16	63	8,185
8GB	**8,456,749,056 bytes**	16,517,088	16	63	16,386

03 Interface Description

The following sections provide detailed information on the Cactus Technologies Industrial SSD interface.

3.1. DOM Pin Assignments and Pin Type

The signal/pin assignments are listed in Table 3-6. Low active signals have a "-" prefix. Pin types are Input, Output or Input/Output. Sections 3.3.1 to 3.3.4 define the DC characteristics for all input and output type structures.

Table 3-6. 40/44 DOM Pin Assignments and Pin Type

Pin Num	Signal Name	Pin Type	Pin Num	Signal Name	Pin Type
1	-Reset	I	2	GND	
3	Data 7	I/O	4	Data 8	I/O
5	Data 6	I/O	6	Data 9	I/O
7	Data 5	I/O	8	Data 10	I/O
9	Data 4	I/O	10	Data 11	I/O
11	Data 3	I/O	12	Data 12	I/O
13	Data 2	I/O	14	Data 13	I/O
15	Data 1	I/O	16	Data 14	I/O
17	Data 0	I/O	18	Data 15	I/O
19	GND		20	Key /Vcc [1]	
21	-DMARQ	O	22	GND	
23	-IOW / STOP	I	24	GND	
25	-IOR/ -HDMARDY/ HSTROBE	I	26	GND	
27	IORDY/ -DDMARDY/ DSTROBE	O	28	-CSEL	I
29	-DMACK	I	30	GND	
31	IRQ	O	32	-IOCS16	O
33	A1	I	34	-PDIAG	I/O
35	A0	I	36	A2	I
37	-CS0	I	38	-CS1	I
39	-DASP	I/O	40	GND	
41	Vcc		42	Vcc	
43	GND		44	Reserved	

Note: Pins 41-44 available on 44pin DOMs only

1: Pin 20 can be used as an alternate Vcc supply input for the 40-pin DOM. If not used as alternate Vcc pin, this pin should be left unconnected.

3.2. Signal Description

Table 3-7 describes the I/O signals. Signals whose source is the host are designated as inputs while signals that the DOM sources are outputs. The DOM logic levels conform to those specified in the ANSI ATA Specification.

Table 3-7. Signal Description

Signal Name	Dir.	Description
A2—A0	I	A[2:0] is used to select the one of eight registers in the Task File.
-PDIAG	I/O	This input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
-DASP	I/O	This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
-CS0, -CS1	I	-CS0 is the chip select for the task file registers while -CS1 is used to select the Alternate Status Register and the Device Control Register.
-CSEL	I	This internally pulled up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.
D15—D00	I/O	These lines carry the Data, Commands and Status information between the host and the controller. D00 is the LSB of the Even Byte of the Word. D08 is the LSB of the Odd Byte of the Word. All Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bits using D00-D15.
GND	--	Ground.
-IORD -HDMARDY HSTROBE	I	When UDMA protocol is not active, this is an I/O Read strobe generated by the host which gates I/O data onto the bus from the DOM. When UDMA Read protocol is active, this signal is asserted by the host to indicate that it is ready to receive data-in bursts. When UDMA Write protocol is active, this signal is the data out strobe sent by the host. Data is latched by the device on both rising and falling edges of this strobe.

Signal Name	Dir.	Description
-IOWR STOP	I	When UDMA protocol is not active, this is the I/O Write strobe pulse which is used to clock I/O data on the Data bus into the DOM. The clocking will occur on the negative to positive edge of the signal (trailing edge). When UDMA protocol is active, this signal is asserted by the host to terminate the UDMA transfer.
INTRQ	O	This signal is the active high Interrupt Request to the host.
-RESET	I	This input pin is the active low hardware reset from the host.
VCC	--	+5 V, +3.3 V power.
-IORDY -DDMARDY DSTROBE	O	When UDMA protocol is not active, this signal is driven by the device to extend the I/O cycle in progress. When UDMA Write protocol is active, this signal is asserted by the device to indicate that it is ready to receive a data-out burst. When UDMA Read protocol is active, this signal is the data strobe sent by the device to the host. The host latches the data on both rising and falling edges of this strobe.
-IOCS16	O	This output signal is asserted low when this device is expecting a word data transfer cycle.
DMARQ	O	This signal is driven by the DOM to request DMA data transfer to/ from the host.
-DMACK	I	This signal is driven by the host in response to a DMA request by the DOM.

3.3. Electrical Specification

The following table defines all D.C. Characteristics for the DOM Series. Unless otherwise stated, conditions are:

Vcc = 5V ± 10% or Vcc = 3.3V ± 10%
Ta = -45°C to 90°C

3.3.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Storage Temperature	Ts	-65	+150	°C
Operating Temperature	T_A	-45	+90	°C
Vcc with respect to GND	Vcc	-0.3	6.5	V

3.3.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Operating Current Sleep Mode Active	I_{cc}		 0,6 280	mA

3.3.3. AC Characteristics

Cactus Technologies DOM meets all the timing requirements as specified in the ATA5 standard. Please refer to the official ATA5 documentation for details on AC Timing diagrams and parameters.

3.4. I/O Transfer Function

Table 3-7defines the function of the operations for the DOM.

Table 3-7 DOM I/O Function

Function Code	-CE2	-CE1	Address	-IORD	-IOWR	D15-D8	D7-D0
Invalid Mode	L	L	X	X	X	High Z	High Z
Standby Mode	H	H	X	X	X	High Z	High Z
Task File Write	H	L	1-7h	H	L	Do not care	Data In
Task File Read	H	L	1-7h	L	H	High Z	Data Out
Data Register Write	H	L	0	H	L	Odd-Byte In	Even-Byte In
Data Register Read	H	L	0	L	H	Odd-Byte Out	Even-Byte Out
Control Register Write	L	H	6h	H	L	Do not care	Control In
Alt Status Read	L	H	6h	L	H	High Z	Status Out

04 ATA Drive Register Set Definition and Protocol

The communication to or from the DOM is done using the Task File registers, which provide all the necessary registers for control and status information. The ATA interface connects peripherals to the host using four register mapping methods. Table 4-8 is a detailed description of these methods.

Table 4-8. I/O Configurations

Address	Drive #	Description
1F0-1F7, 3F6-3F7	0	Primary I/O Mapped Drive 0
1F0-1F7, 3F6-3F7	1	Primary I/O Mapped Drive 1
170-177, 376-377	0	Secondary I/O Mapped Drive 0
170-177, 376-377	1	Secondary I/O Mapped Drive 1

4.1. Task File Addressing

I/O decoding to access the task file registers is as listed in Table 4-9.

Table 4-9. Task File I/O Decoding

-CE2	-CE1	A2	A1	A0	-IORD=0	-IOWR=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error Register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Drive/Head	Select Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control
0	1	1	1	1	Drive Address	Reserved

4.2. ATA Registers

4.2.1. Data Register (Address-1F0[170])

The Data Register is a 16-bit register, and it is used to transfer data blocks between the DOMdata buffer and the Host.

4.2.2. Error Register (Address-1F1[171]; Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.

Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.

Bit 5 This bit is 0.

Bit 4 (IDNF) The requested sector ID is in error or cannot be found.

Bit 3 This bit is 0.

Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.

Bit 1 This bit is 0.

Bit 0 (AMNF) This bit is set in case of a general error.

4.2.3. Feature Register (Address-1F1[171]; Write Only)

This register provides information regarding features of the DOM that the host can utilize.

4.2.4. Sector Count Register (Address-1F2[172])

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the DOM. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

4.2.5. Sector Number (LBA 7-0) Register (Address-1F3[173])

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any DOM data access for the subsequent command.

4.2.6. Cylinder Low (LBA 15-8) Register (Address-1F4[174])

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

4.2.7. Cylinder High (LBA 23-16) Register (Address-1F5[175])

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

4.2.8. Drive/Head (LBA 27-24) Register (Address 1F6[176])

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.

Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.

Bit 5 This bit is set to 1.

Bit 4 (DRV) This bit will have the following meaning. DRV is the drive number. When DRV=0, drive 0 is selected When DRV=1, drive 1 is selected.

Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.

Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.

Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.

Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

4.2.9. Status and Alternate Status Registers (Address 1F7[177] and 3F6[376])

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.

Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.

Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.

Bit 4 (DSC) This bit is set when the device is ready.

Bit 3 (DRQ) The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.

Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.

Bit 1 (IDX) This bit is always set to 0.

Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

4.2.10. Device Control Register (Address-3F6[376])

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is an X (Do not care).

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the drive.

Bit 2 (SW Rst) This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the drive.

4.2.11. Drive Address Register (Address 3F7[377])

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.
Implementation Note:
Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the DOM. Following are some
possible solutions to this problem:
1. Locate the DOM at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a DOM in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a DOM product is installed and conversely to tri-state D6 D0
of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the DOM's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the DOM or b) if provided use an additional Primary/Secondary configuration in the DOM that does not respond to accesses to I/O locations 3F7 and 377.
With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

05 ATA Command Description

Table 5-10 summarizes the supported ATA command set.

Table 5-10. ATA Command Set

COMMAND	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5h or 98h	-	-	-	-	D	-
Execute Drive Diagnostic	90h	-	-	-	-	-	-
Erase Sector(s)	C0h	-	Y	Y	Y	Y	Y
Format Track	50h	-	Y	-	Y	Y	Y
Identify Drive	ECh	-	-	-	-	D	-
Idle	E3h or 97h	-	Y	-	-	D	-
Idle Immediate	E1h or 95h	-	-	-	-	D	-
Initialize Drive Parameters	91h	-	Y	-	-	Y	-
Read Buffer	E4h	-	-	-	-	D	-
Read Multiple	C4h	-	Y	Y	Y	Y	Y
Read Long Sector	22h or 23h	-	-	Y	Y	Y	Y
Read Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
Read Verify Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
Recalibrate	1Xh	-	-	-	-	D	-
Request Sense	03h	-	-	-	-	D	-
Seek	7Xh	-	-	Y	Y	Y	Y
Set Features	EFh	Y	-	-	-	D	-
Set Multiple Mode	C6h	-	Y	-	-	D	-
Set Sleep Mode	E6h or 99h	-	-	-	-	D	-
Stand By	E2h or 96h	-	-	-	-	D	-
Stand By Immediate	E0h or 94h	-	-	-	-	D	-
Translate Sector	87h	-	Y	Y	Y	Y	Y
Wear Level	F5h	-	-	-	-	Y	-
Write Buffer	E8h	-	-	-	-	D	-
Write Long Sector	32h or 33h	-	-	Y	Y	Y	Y
Write Multiple	C5h	-	Y	Y	Y	Y	Y
Write Multiple w/o Erase	CDh	-	Y	Y	Y	Y	Y
Write Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
Write Sector(s) w/o Erase	38h	-	Y	Y	Y	Y	Y
Write Verify Sector(s)	3Ch	-	Y	Y	Y	Y	Y

Definitions: FR = Features Register, SC = Sector Count Register, SN = Sector Number Register, CY = Cylinder Registers, DH = Drive/Drive/Head Register, LBA = Logical Block Address Mode Supported (see command descriptions for use).

Y—The register contains a valid parameter for this command. For the Drive/Head Register Y means both the drive and head parameters are used; D—only the drive parameter is valid and not the head parameter.

5.1. Identify Drive-ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-11. All reserved bits or words are zero. Table 5-11 is the definition for each field in the Identify Drive Information.

Word Address	Default Value	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit-significant information.
1	XXXXH	2	Default number of cylinders; capacity dependent.
2	0000H	2	Reserved.
3	00XXH	2	Default number of heads; capacity dependent.
4	0000H	2	Number of unformatted bytes per track.
5	0200H	2	Number of unformatted bytes per sector.
6	00XXH	2	Default number of sectors per track; capacity dependent.
7-8	XXXXH,XXXXH	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW); capacity dependent.
9	0000H	2	Reserved.
10-19	aaaa	20	Serial number in ASCII (Right Justified).
20	0002H	2	Buffer type (dual port).
21	000XH	2	Buffer size in 512 byte increments. 0001H for 1GB or below; 0002H for 2GB or above.
22	0004H	2	Number of ECC bytes passed on Read/Write Long Commands.
23-26	aaaa	8	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	aaaa	40	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	800XH	2	
48	0000H	2	Double Word not supported.
49	0F00H	2	Capabilities: DMA Supported in True IDE mode (bit 8), LBA supported (bit 9).
50	0000H	2	Reserved.
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Single Word DMA data transfer cycle timing mode (not supported).
53	0007H	2	Data fields 54-58,64-70 and 88 are valid.
54	XXXX	2	Current numbers of cylinders.
55	XXXX	2	Current numbers of heads.

Word Address	Default Value	Total Bytes	Data Field Type Information
56	XXXX	2	Current sectors per track.
57-58	XXXX	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW).
59	010XH	2	Multiple sector setting is valid; low byte is capacity dependent.
60-61	XXXX	4	Total number of sectors addressable in LBA Mode.
62	0000H	2	Reserved
63	0X07H	2	Multiword DMA modes 0-2 are supported; upper byte reflects currently selected MWDMA mode.
64	0003H	2	Advanced PIO modes supported (modes 3 and 4)
65	0078H	2	Minimum MWDMA cycle time per word is 120ns.
66	0078H	2	Recommended MWDMA cycle time is 120ns.
67	0078H	2	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	2	Minimum PIO cycle time with IORDY flow control is 120ns.
69-79	-	22	Reserved
80	0020H	2	Supports ATA5 standard.
81	0000H	2	No minor revision reported.
82	740H	2	Read/Write Buffer command supported; host protected area supported; PACKET Command, Security Mode and SMART feature sets not supported;
83	5000H	2	48-bit mode not supported; CFA feature set not supported.
84	4000H	2	Features defined in this word not supported.
85	7408H	2	Read/Write Buffer, host protected area and Power Management features enabled.
86	1000H	2	CFA Feature set not enabled.
87	4000H	2	Features defined by this word not enabled.
88	XX1FH	2	UDMA Modes 0-4 supported.
89-99	0000H	22	Reserved
100-103	XXXXH	8	Maximum user LBA for 48-bit addressing mode (not used).
104-255	-		Reserved

Model KMXFY-303Z

Where X is card capacities:

128M	128MB
256M	256MB
512M	512MB
1G	1GB
2G	2GB
4G	4GB
8G	8GB

Where Y is temperature

Blank	Standard temperature (0° C to +70° C)
I	Extended temperature (-45° C to +90° C)

Where Z is form factor

AV	40-Pin vertical
AR	40-Pin horizontal right
AL	40-Pin horizontal left
BV	44-Pin vertical
BR	44-Pin horizontal right
BL	44-Pin horizontal left

Example:

1. 512MB 40-Pin vertical DOM KM512MF-303AV
2. 1GB 44-Pin horizontal right DOM Extended Temp KM1GFI-303BR
3. 2GB 40-Pin vertical DOM KM2GF-303AV
4. 128MB 44-Pin horizontal left DOM Extended Temp KM128MFI-303BL

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Appendix D Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its Industrial Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for five years from the date of purchase. This express warranty is extended by Cactus Technologies® Limited

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies®' responsibilities regarding the Cactus Industrial Grade DOM products. In satisfaction of its obligations hereunder, Cactus Technologies®, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

Cactus Technologies®' products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within five years of purchase, Cactus Technologies® will have the option of repairing or replacing the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product s functional and performance specifications. Upon confirmation of

failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

Cactus Technologies® reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

Cactus Technologies® may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, Cactus Technologies® also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product s specifications.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

Cactus Technologies® Limited
Suite C, 15/F, Capital Trade Center
62 Tsun Yip Street, Kwun Tong
Kowloon, Hong Kong