OEM Grade
-255SH series
SSD

Product Manual

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1.Introduction to Cactus Technologies® OEM Grade -255SH Series SSD Products

Features:

- Solid state design with no moving parts
- Available in industry standard 2.5” 9.5mm height form factor
- Capacities: 2TB
- Compliant with Serial ATA 3.0 specifications
- ATA8-ACS2 command set compatible
- Supports Serial ATA Generation I/II/III transfer rate of 1.5/3.0/6.0Gbps
- Supports ATA SMART Feature Set
- Supports ATA Security Feature Set
- Supports Data Set Management Trim command
- Supports SATA NCQ with max. Queue depth of 32
- Enhanced error correction, < 1 error in 10^{15} bits read
- SATA partial and slumber modes supported
- Voltage support: 5.0V±10%

Cactus Technologies® -255SH series SSD is a high capacity solid-state flash memory product that complies with the Serial ATA 3.0 standard and is functionally compatible with a SATA hard disk drive. Cactus Technologies® -255SH series SSD provides up to 2TB of formatted storage capacity.

Cactus Technologies® -255SH series SSD product uses high quality MLC HLNAND flash memory from Hynix Corporation operating in pSLC mode, thus offering improved endurance as compared to standard MLC NAND. In addition, it includes an on-drive intelligent controller that manages interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics, power management, and clock control. The controller’s firmware is upgradeable, thus allowing feature enhancements and firmware updates while keeping the BOM stable.

1.1. Supported Standards

Cactus Technologies® -255SH series SSD is fully compatible with the following specification:

- ATA 8 Specification published by ANSI
- Serial ATA 3.0 Specification published by the Serial ATA International Organization

1.2. Product Features

Cactus Technologies® OEM SSD contains a high level, intelligent controller. This intelligent controller provides many capabilities including the following:

- Standard ATA register and command set (same as found on most magnetic disk drives).
- Manages details of erasing and programming flash memory independent of the host system
- Sophisticated defect managing capabilities (similar to magnetic disk drives).
- Sophisticated system for error recovery using powerful error correction code (ECC).
- Intelligent power management for low power operation.

1.2.1. Host and Technology Independence

Cactus Technologies® OEM SSD appears as a standard SATA disk drive to the host system. The drive utilizes a 512-byte sector which is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host computer software simply issues an ATA Read or Write command to the drive as per the SATA protocol. The host software then waits for the command to complete. The host system does not get involved in the details of how the flash memory is erased, programmed or read as this is all managed by the built-in controller in the drive. Also, with the intelligent on-board controller, the host system software will not require changing as new flash memory evolves. Thus, systems that support the Cactus Technologies® OEM SSD products today will continue to work with future Cactus Technologies® OEM SSDs built with new flash technology without having to update or change host software.

1.2.2. Defect and Error Management

Cactus Technologies® OEM SSD contains a sophisticated defect and error management system similar to those found in magnetic disk drives. The defect management is completely transparent to the host and does not consume any user data space.

The soft error rate for Cactus Technologies® OEM SSD is much lower than that of magnetic disk drives. In the extremely rare case where a read error does occur, the drive has sophisticated ECC to recover the data.

These defect and error management systems, coupled with the solid-state construction, give Cactus Technologies® OEM SSDs unparalleled reliability.

1.2.3. Power Supply Requirements

Cactus Technologies® OEM SSD operates at a voltage range of 5.0 volts ± 10%.

2.Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. Environmental Specifications

		Cactus Technologies® -255SH SSD
Temperature	Operating:	-40° C to +85° C
Humidity	Operating & Non-Operating:	8% to 95%, non-condensing
Vibration	Operating & Non-Operating:	16.3G RMS (10-2000Hz)
Shock	Operating & Non-Operating:	1,000 G/0.5ms
Altitude (relative to sea level)	Operating & Non-Operating:	100,000 feet maximum

2.2. System Power Requirements

Table 2-2. Power Requirements

		Cactus Technologies® -255SH SSD
DC Input Voltage (VCC) 100 mV max. ripple (p-p)		5.0V ±10%
(Maximum Average Value) See Notes.	Standby: Reading: Writing:	435mA 685mA 805mA

NOTES: All values quoted are typical at ambient temperature and nominal supply voltage unless otherwise stated.

Sleep mode is specified under the condition that all drive inputs are static CMOS levels and in a “Not Busy“ operating state.

2.3. System Performance

All performance timings assume the drive controller is in the default (i.e., fastest) mode.

Table 2-3. Performance

Read Transfer Rate	Sequential (128KB)	Up to 520MBytes/sec
Write Transfer Rate	Sequential (128KB)	Up to 500MBytes/sec
IOPS	4K random read 4K random write	Up to 40K Up to 50K

.

2.4. System Reliability

Table 2-4. Reliability

Data Reliability	< 1 non-recoverable error in 10^{15} bits READ
Endurance (TBW):	2TB: Up to 5PB 4TB: Up to 10PB

Note: TBW rating is estimated based on 128KB sequential write workload; the rating could be lower for other types of workload.

2.5. Physical Specifications

The following sections provide the physical specifications for Cactus Technologies® OEM SSD products.

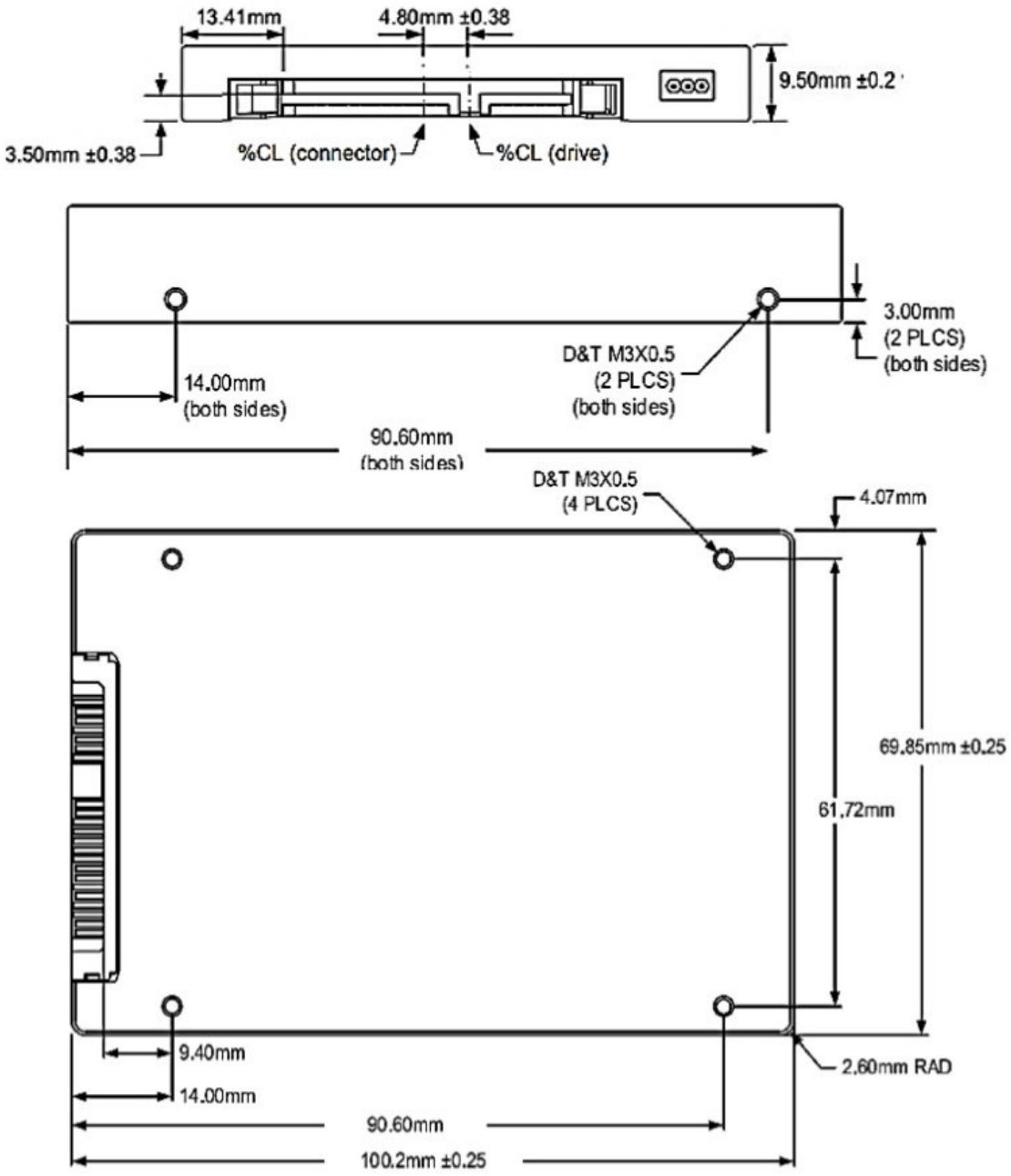
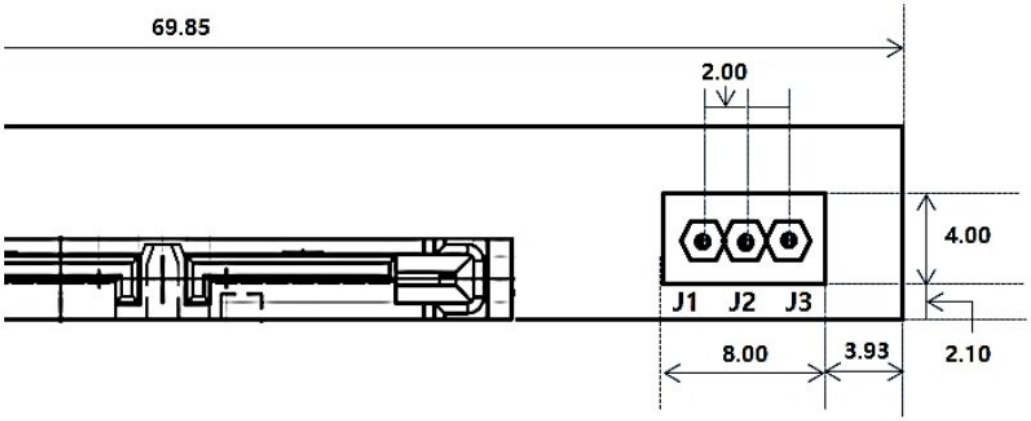


Figure 2-1. 255S 2.5” SSD Dimensions

3.Jumper Options



The functions triggered by the jumper are defined as follows:

Jumper Option	Function
Short J1 to J2	Write Protect
Short J3 to J2	Trigger Erase protocol. The supported protocols are: • quick erase (default) • DoD 5220 22-M NISPOM • DoD 5220 22-M NISPOM, Sup 1 • IRIG 106-07 • NSA 130-2 • NISPOMSUP Chap 8, Sect. 8-501 • Army AR 380-19 • Navy NAVSO P-5239-26 • Air Force AFSSI 5020 • NSA 9-12

Parts with jumper option enabled will be assigned a special -XX suffix, please contact your Cactus Technologies® sales representative for the appropriate suffix to use.

4.Interface Description

The following sections provide detailed information on the Cactus Technologies® OEM SSD interface.

4.1. SSD Pin Assignments and Pin Type

Cactus Technologies® SSD uses industry standard 7+12 SATA connector. The signal/pin assignments and descriptions are listed in Table 3-5.

Table 3-5. SSD Pin Assignments and Pin Type

Signal Segment Pin #	Signal Name	Pin Type
S1	GND	
S2	RXP	Analog In
S3	RXN	Analog In
S4	GND	
S5	TXN	Analog Out
S6	TXP	Analog Out
S7	GND	

Power Segment Pin #	Signal Name	Pin Type
P1	NC	
P2	NC	
P3	NC	
P4	GND	
P5	GND	
P6	GND	
P7	5V	
P8	5V	
P9	5V	
P10	GND	
P11	Active LED	
P12	GND	
P13	12V	
P14	12V	
P15	12V	

4.2. Electrical Specifications

The following table defines all D.C. Characteristics for the SSD products. Unless otherwise stated, conditions are:

Vcc = 5.0V ± 10%
Ta = -40°C to 85°C

4.2.1. Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units
Operating Temperature	Ts	-40	+85	°C
Storage Temperature	T_A	-55	+100	°C
Vcc with respect to GND	Vcc	-0.3	5.5	V

4.2.2. DC Characteristics

Parameter	Symbol	MIN	MAX	Units
Input Voltage	Vin	-0.5	Vcc + 0.5	V
Output Voltage	Vout	-0.3	Vcc + 0.3	V
Input Leakage Current	I_{LI}	-10	10	uA
Output Leakage Current	I_{LO}	-10	10	uA
Input/Output Capacitance	C_I/C_o		10	pF
Power Consumption (avg) Idle Active	Pavg		 445 1080	mA

4.2.3. AC Characteristics

Cactus Technologies® OEM SSD products conforms to all AC timing requirements as specified in the SATA-IO specifications. Please refer to that document for details of AC timing for all operation modes of the device.

5.ATA Drive Register Set Definition and Protocol

The communication to or from the SSD is done using FIS. Legacy ATA protocol is supported by using the legacy mode defined in the SATA specifications. In this mode, the FIS has defined fields which provide all the necessary ATA task file registers for control and status information. The Serial ATA interface does not support Primary/Secondary or Master/Slave configurations. Each SATA channel supports only one SATA device, with the register selection as defined by the ATA standard.

5.1. ATA Task File Definitions

The following sections describes the usage of the ATA task file registers. Note that the Alternate Status Register of legacy ATA is not defined for SATA drives.

5.1.1. Data Register

The Data Register is a 16-bit register, and it is used to transfer data blocks between the SSD data buffer and the Host.

5.1.2. Error Register

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Bit 7 (BBK) This bit is set when a Bad Block is detected.
Bit 6 (UNC) This bit is set when an Uncorrectable Error is encountered.
Bit 5 This bit is 0.
Bit 4 (IDNF) The requested sector ID is in error or cannot be found.
Bit 3 This bit is 0.
Bit 2 (Abort) This bit is set if the command has been aborted because of a status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued.
Bit 1 This bit is 0.
Bit 0 (AMNF) This bit is set in case of a general error.

5.1.3. Feature Register

This register provides information regarding features of the SSD that the host can utilize.

5.1.4. Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the SSD. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

5.1.5. Sector Number (LBA 7-0) Register

This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any SSD data access for the subsequent command.

5.1.6. Cylinder Low (LBA 15-8) Register

This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

5.1.7. Cylinder High (LBA 23-16) Register

This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

5.1.8. Drive/Head (LBA 27-24) Register

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7 This bit is set to 1.
Bit 6 LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address Mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block Mode, the Logical Block Address is interpreted as follows:
LBA07-LBA00: Sector Number Register D7-D0.
LBA15-LBA08: Cylinder Low Register D7-D0.
LBA23-LBA16: Cylinder High Register D7-D0.
LBA27-LBA24: Drive/Head Register bits HS3-HS0.
Bit 5 This bit is set to 1.
Bit 4 (DRV) DRV is the drive number. This should always be set to 0.
Bit 3 (HS3) When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2) When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1) When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0) When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

5.1.9. Status Registers

These registers return the status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (BUSY) The busy bit is set when the device has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
Bit 6 (RDY) RDY indicates whether the device is capable of performing operations requested by the host. This bit is cleared at power up and remains cleared until the device is ready to accept a command.
Bit 5 (DWF) This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC) This bit is set when the device is ready.
Bit 3 (DRQ) The Data Request is set when the device requires that information be transferred either to or from the host through the Data register.
Bit 2 (CORR) This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1 (IDX) This bit is always set to 0.
Bit 0 (ERR) This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error.

5.1.10. Device Control Register

This register is used to control the drive interrupt request and to issue an ATA soft reset to the drive. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
HOB	X	X	X	1	SW Rst	-IEn	0

Bit 7 This bit is used in 48-bit addressing mode. When cleared, the host can read the most recently written values of the Sector Count,Drive/Head and LBA registers. When set, the host will read the previous written values of these registers. A write to any Command block register will clear this bit.

Bit 6 This bit is an X (Do not care).

Bit 5 This bit is an X (Do not care).

Bit 4 This bit is an X (Do not care).

Bit 3 This bit is ignored by the drive.

Bit 2 (SW Rst) This bit is set to 1 in order to force the drive to perform an AT Disk controller Soft Reset operation. The drive remains in Reset until this bit is reset to '0'.

Bit 1 (-IEn) The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the drive are disabled. This bit is set to 0 at power on and Reset.

Bit 0 This bit is ignored by the drive.

5.1.11. Drive Address Register

This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0

Bit 7 This bit is unknown.

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the SSD. Following are some possible solutions to this problem:

1. Locate the SSD at a non-conflicting address (i.e., Secondary address (377) when a Floppy Disk Controller is located at the Primary addresses).
2. Do not install a Floppy and a SSD in the system at the same time.
3. Implement a socket adapter that can be programmed to (conditionally) tri-state D7 of I/0 address 3F7/377 when a SSD product is installed and conversely to tri-state D6-D0 of I/O address 3F7/377 when a floppy controller is installed.
4. Do not use the SSD’s Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0-1F7, 3F6 (or 170-177, 176) to the SSD or b) if provided use an additional Primary/Secondary configuration in the SSD that does not respond to accesses to I/O locations 3F7 and 377. With either of these implementations, the host software must not attempt to use information in the Drive Address Register.

Bit 6 (-WTG) This bit is 0 when a write operation is in progress, otherwise, it is 1.

Bit 5 (-HS3) This bit is the negation of bit 3 in the Drive/Head register.

Bit 4 (-HS2) This bit is the negation of bit 2 in the Drive/Head register.

Bit 3 (-HS1) This bit is the negation of bit 1 in the Drive/Head register.

Bit 2 (-HS0) This bit is the negation of bit 0 in the Drive/Head register.

Bit 1 (-nDS1) This bit is 0 when drive 1 is active and selected.

Bit 0 (-nDS0) This bit is 0 when the drive 0 is active and selected.

6.ATA Command Description

This section defines the ATA command set supported by Cactus Technologies® -255SH series SSDs.

6.1. ATA Command Set

Table 5-6 summarizes the supported ATA command set .

Table 5-6. ATA Command Set

COMMAND	Code
Check Power Mode	E5h, 98h
Device Reset	08h
Device Configuration	-
Device Configuration Freeze Lock	B1h/C1h
Device Configuration Identify	B1h/C2h
Device Configuration Restore	B1h/C0h
Device Configuration Set	B1h/C3h
Download Microcode	92h
Data Set Management	06h
Execute Drive Diagnostic	90h
Flush Cache	E7h
Flush Cache Ext	EAh
Identify Drive	ECh
Idle	E3h, 97h
Idle Immediate	E1h, 95h
Initialize Drive Parameters	91h
Read Buffer	E4h
Read DMA	C8h
Read DMA Ext	25h
Read FDPMA Queued	60h
Read Log Ext	2Fh
Read Multiple	C4h
Read Multiple Ext	29h
Read Native Max Address	F8h
Read Native Max Address Ext	27h
Read Sector(s)	20h
Read Sector(s) Ext	24h
Read Verify Sector(s)	40h
Read Verify Sector(s) Ext	42h
Security Disable Password	F6h
Security Erase Prepare	F3h
Security Erase Unit	F4h
Security Freeze Lock	F5h
Security Set Password	F1h
Security Unlock	F2h
Seek	70h
Set Features *	EFh
Enable Write Cache	Efh/02h

COMMAND	Code
Disable Write Cache	EFh/82h
Set Transfer Mode	EFh/03h
Enable Power-up In Standby	EFh/06h
Disable Power-up In Standby	EFh/86h
Enable DMA Setup FIS Auto-Activate optimization	EFh/10h/02h
Disable DMA Setup FIS Auto-Activate optimization	EFh/90h/02h
Enable Device-initiated interface power state transitions	EFh/10h/03h
Disable Device-initiated interface power state transitions	EFh/90h/03h
Set Max	
Set Max Address	F9h
Set Max Freeze Lock	F9h/04h
Set Max Lock	F9h/02h
Set Max Set Password	F9h/01h
Set Max Unlock	F9h/03h
Set Max Address Ext	37h
Set Multiple Mode	C6h
Set Sleep Mode	E6h, 99h
SMART	
SMART Disable Operations	B0h/D9h
SMART Enable Operations	B0h/D8h
SMART Enable/Disable Attribute Autosave	B0h/D2h
SMART Execute Off-line Immediate	B0h/D4h
SMART Read Attribute Thresholds	B0h/D1h
SMART Read Data	B0h/D0h
SMART Read Log	B0h/D5h
SMART Return Status	B0h/DAh
SMART Save Attribute Values	B0h/D3h
SMART Write Log	B0h/D6h
Stand By	E2h, 96h
Stand By Immediate	E0h, 94h
Soft Reset	FFh
Write Buffer	E8h
Write DMA	CAh
Write DMA Ext	35h
Write FPDMA Queued	61h
Write Log Ext	3Fh
Write Multiple	C5h
Write Multiple Ext	39h
Write Sector(s)	30h
Write Sector(s) Ext	34h

6.1.1. Identify Drive—ECH

The Identify Drive command enables the host to receive parameter information from the drive. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 5-7. All reserved bits or words are zero. Table 5-7 is the definition for each field in the Identify Drive Information.

Table 5-7. Identify Drive Information

Word Address	Default Value	Data Field Type Information
0	0040H	General configuration bit-significant information.
1	3FFFH	Default number of cylinders; capacity dependent.
2	C837H	Reserved
3	0010H	Default number of heads; capacity dependent.
4-5	0H	Retired
6	003FH	Default number of sectors per track; capacity dependent.
7-8	0h	Reserved
9	0H	Retired
10-19	varies	Serial number in ASCII (Right Justified).
20-21	0H	Retired
22	0H	Obsolete
23-26	varies	Firmware revision in ASCII . Big Endian Byte Order in Word.
27-46	varies	Model number in ASCII (Left Justified) Big Endian Byte Order in Word.
47	8001H	Maximum number of sectors on Read/Write Multiple command: 2
48	4000H	Trusted Computing Feature Set
49	2F00H	Capabilities: DMA, LBA, IORDY supported
50	4000H	Capabilities: device specific standby timer minimum
51	0H	Obsolete
52	0H	Obsolete
53	0007H	Words 88 and 70:64 valid
54	3FFFH	Obsolete
55	0010H	Obsolete
56	003FH	Obsolete
57-58	0H	Obsolete
59	0101H	Number of sectors transferred per interrupt
60-62	varies	Total number of sectors addressable
63	0407H	Multiword DMA modes 0-2 are supported; upper byte reflects currently selected MWDMA mode.
64	0003H	Advanced PIO modes supported (modes 3 and 4)
65	0078H	Minimum MWDMA cycle time per word is 120ns.
66	0078H	Recommended MWDMA cycle time is 120ns.
67	0078H	Minimum PIO cycle time without IORDY flow control is 120ns.
68	0078H	Minimum PIO cycle time with IORDY flow control is 120ns.
69	4020H	Additional features supported
70	0H	Reserved
71-74	0H	Reserved
75	001FH	Queue depth of 32 for NCQ
76	050EH	SATA capabilities
77	0006H	Reserved
78	0044H	Support of SerialATA functions
79	0044H	Serial ATA functions enabled

Word Address	Default Value	Data Field Type Information
80	01E0H	Major revision number
81	0000H	Minor revision number
82	346BH	Command set supported
83	7D01H	Command set supported
84	4122H	Command set/feature supported extension
85	3469H	Command set/feature enabled
86	3C01H	Command set/feature enabled
87	4122H	Command set/feature default
88	007FH	UDMA Modes 0-6 supported.
89	0004H	Time required for security erase unit completion
90	0004H	Time required for enhanced security erase unit completion
91	0000H	Current advanced power management value
92	FFFEH	Master password revision code
93	0H	Hardware reset default
94	0H	Vendor's recommended acoustic management value
95	0H	Stream minimum request size
96	0H	Streaming transfer time - DMA
97	0H	Streaming access latency
98-99	0H	Streaming performance granularity
100-103	varies	Maximum user LBA for 48-bit addressing mode.
104	0H	Streaming transfer time - PIO
105	0001H	Max. number of 512-byte blocks of LBA Range Entries per DataSet Management command
106	4000H	Physical sector size per sector
107	0H	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	varies	Unique ID
112-115	0H	Reserved
116	0H	Reserved
117-118	0H	Words per logical sector
119	0H	Features implemented (supported)
120	0H	Features implemented (enabled)
121-126	0H	Reserved
127	0H	Removable Media Status Notification feature set support
128	0001H	Security status
129-159	00H	Vendor specific
160	0H	CFA power mode 1
161-167	0H	Reserved for CFA
168	0003H	Reserved for CFA
169	0001H	Data Set Management Trim attribute support
170-175	0H	Reserved for CFA
176-205	0H	Current media serial number
206	0H	SCT Command Transport
207-208	0H	Reserved
209	4000H	Alignment of logical blocks within a physical block
210-211	0H	Write-Read-Verify Sector Count Mode 3
212-213	0H	Write-Read-Verify Sector Count Mode 2
214	0H	NV Cache Capabilities
215-216	0H	NV Cache Size in Logical Blocks
217	0001H	Nominal media rotational rate
218	0H	Reserved
219	0H	NV Cache Options
220	0H	Write-Read-Verify feature set
221	0H	Reserved
222	103FH	Transport major version number
223	0H	Transport minor version number
224-229	0H	Reserved

Word Address	Default Value	Data Field Type Information
230-233	0H	Extended Number of User Addressable Sectors
234	0H	Min. number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03H
235	0H	Max. number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03H
236-254	0H	Reserved
255	varies	Checksum

7. S.M.A.R.T. Feature Set

Cactus Technologies® -255SH Series SSDs supports S.M.A.R.T. attribute reporting. This following subcommands are supported when programmed into the Feature Register:

Value	Command	Value	Command
D0h	Read Data	D6h	SMART Write Log
D2h	Enable/Disable Autosave	D8h	Enable SMART operations
D4h	Execute OFF-LINE Immediate	D9h	Disable SMART operations
D5h	SMART Read Log	DAh	Return Status

7.1. S.M.A.R.T Data Structure

The Read Data commands returns 512 bytes of data in the following structure:

Byte(s)	Description
0-1	Revision code
2-361	Data for atrributes 1 - 30
362	Off-line data collection status
363	Self-test execution status byte
364-365	Total time in seconds to complete off-line data collection activitiies
366	Vendor specific
367	Off-line data collection capabilities
368-369	SMART capabilities
370	Error logging capabilities: bit[7:1] – reserved: bit[0]: 1=device error logging supported
371	Vendor specific
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374-510	Reserved
511	Data structure checksum

7.2. S.M.A.R.T Attribute Data Structure

Each attribute returned in bytes 2-361 of the 512-byte SMART data has the following format:

Byte(s)	Descriptions
0	Attribute ID
1 – 2	Flags
3	Current Value
4	Worst Value
5 – 10	Attribute value
11	Reserved

7.3. S.M.A.R.T Attributes

The S.M.A.R.T attributes returned by the Read Data command are listed below:

Attribute ID	Attribute Name	Description
01h	Vendor Specific	
09h	Power-on hours	Total time of power-on state in hours
0Ch	Power cycle count	Number of power on/off cycles
0Dh	Vendor Specific	
AFh	Program Failure Block Count	Number of flash program failures bit[23:0]: program fail count; bit[47:24]: erase fail count
B8h	Initial bad block count	Number of initial bad blocks detected during firmware install
BBh	Read Failure Block Count (Uncorrectable)	Uncorrectable read failure block count bit[23:0]: read bad block count; bit[47:24]: potential read bad block count
BEh	Temperature	Current device temperature (°C)
C7h	SATA CRC Error Count	Number of SATA interface errors: bit[23:0]: CRC error count; bit[47:24]: handshake error count
C8h	Total Write count	Total number of write commands issued

Attribute ID	Attribute Name	Description
C9h	Total Read count	Total number of read commands issued
CAh	Vendor Specific	
CCh	Vendor Specific	
D1h	SSD life remaining	Approximate SSD life left (Max. PE cycle – avg. Erase count) / Max. PE cycle
D2h	Erase count	bit[15:0]: min. erase count bit{31:16]: avg. erase count bit[47:32]: max. erase count
D5h	Max. PE count	Maximum allowed Program/Erase count
E1h	Vendor Specific	
E2h	Flush Command Count	Flush command count. bit[23:0]: self flush count bit[47:24]: host flush count
E3h	Vendor Specific	
E4h	Vendor Specific	
E5h	Vendor Specific	
E6h	Total Free Block	The current number of total free blocks count
F1h	Vendor Specific	

7.4. S.M.A.R.T Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to start the off-line process for the requested mode and operation. The LBA Low register shall be set to specify the operation to be executed as follows:

LBA Low value	Description
00h	Execute SMART off-line data collection routine immediately
01h	Execute SMART short self-test routine immediately in off-line mode
02h	Execute SMART Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute SMART Selective self-test routine immediately in off-line mode

LBA Low value	Description
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute SMART short self-test routine immediately in captive mode
82h	Execute SMART Extended self-test routine immediately in captive mode
84h	Execute SMART Selective self-test routine immediately in captive mode
C0h	Reserved

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte and ATA registers and then executes the command completion. Taskfile registers will have return values as follows:

STATUS reg: Set ERR to one when self-test failed

ERR reg: Set ABRT to one when self-test failed

LBA LOW reg: Set to F4h when self-test failed

LBA HIGH reg: Set to 2Ch when self-test failed

7.5. S.M.A.R.T Read Log (subcommand D5h)

This command returns the specified log sector content to the host. LBA Low and Sector Count registers shall be set to specify the log sector and sector number to be written.

LBA Low value	Sector Count	Content	
00h	1	Log directory	Read only
01h	1	SMART error log	Read only
02h	51	Comprehensive SMART error log	Read only
03h	37	Extended Comprehensive SMART error log	Read only
06h	1	SMART self-test log	Read only
07h	1	Extended SMART self-test log	Read only
09h	1	Selective self-test log	R/W

LBA Low value	Sector Count	Content	
10h	1	NCQ error log	Read only
11h	1	SATA PHY event counter log	Read only
80h-9Fh	32	Host vendor specific	R/W
A0h	1	Reserved	Vendor Specific

7.5.1. S.M.A.R.T Log Directory Structure

Byte(s)	Description
0-1	SMART log version (set to 01h)
2-3	Number of sectors in the log at log address 1
4-5	Number of sectors in the log at log address 2
6-509	Number of sector in the log at log addresses 3 to 254
510-511	Number of sectors in the log at log address 255

7.5.2. Self-test Log Structure

Byte(s)	Description
0-1	Log version
2+n*24	Self-test number
3+n*24	Self-test status
4+n*24 - 5+n*24	timestamp
6+n*24	Self-test failure checkpoint
7+n*24 - 10+n*24	LBA of first failure
11+n*24 - 25+n*24	Vendor specific
----	----
506-507	Vendor specific
508	Self-test log pointer
509-510	Reserved
511	Checksum

n is 0 through 20.

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

7.5.3. SelectiveSelf-test Log Structure

Byte(s)	Description	Read/Write
0-1	Log version	R/W
2-9	Starting LBA for test span 1	R/W
10-17	Ending LBA for test span 1	R/W
18-25	Starting LBA for test span 2	R/W
26-33	Ending LBA for test span 2	R/W
34-41	Starting LBA for test span 3	R/W
42-49	Ending LBA for test span 3	R/W
50-57	Starting LBA for test span 4	R/W
58-65	Ending LBA for test span 4	R/W
66-73	Starting LBA for test span 5	R/W
74-81	Ending LBA for test span 5	R/W
82-337	Reserved	--
338-491	Vendor specific	--
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags R/W	R/W
504-507	Vendor specific	--
508-509	Selective self test pending time	R/W
510	Reserved	--
511	Checksum	R/W

7.6. S.M.A.R.T Write Log Sector (subcommand D6h)

This subcommand writes 512 bytes of data to the specified log sector. LBA Low and Sector Count registers shall be set to specify the log address and sector number to be written.

7.7. S.M.A.R.T Enable Operations (subcommand D8h)

This subcommand enables access to all SMART capabilities. Prior to issuance of this subcommand, SMART attributes are not being monitored. The state of SMART, whether enabled or disabled, is preserved across power cycling.

7.8. S.M.A.R.T Disable Operations (subcommand D9h)

This subcommand disables all SMART capabilities. After receipt of this subcommand, all other SMART commands other than SMART Enable operations will be aborted and error code returned. SMART attributes that are being monitored while SMART operation is enabled will be saved. If SMART operation is enabled subsequently, the attribute values will be updated accordingly.

7.9. S.M.A.R.T Return Status (subcommand DAh)

This subcommand returns the reliability status of the device to the host. Upon receipt of this command, the device saves any updated Attribute values to the reserve sector and compares the updated Attribute values to preset Attribute thresholds.

Appendix A. Ordering Information

Model KDXFI-255SH-YY

Where: X is drive capacities:

2T ---------- 2TB

Where: YY is jumper option

Consult with Cactus Technologies® sales for jumper option assignments.

Example:

(1) 2TB 2.5” SSD ---------- KD2TFI-255SH

Appendix B.Technical Support Services

B.1.Direct Cactus Technologies® Technical Support

Email: tech@cactus-tech.com

Appendix C.Cactus Technologies® Worldwide Sales Offices

Email: sales@cactus-tech.com

Email: americas@cactus-tech.com

Appendix D.Limited Warranty

I. WARRANTY STATEMENT

Cactus Technologies® warrants its OEM Grade products only to be free of any defects in materials or workmanship that would prevent them from functioning properly for two years from the date of purchase or when rated TBW is reached, whichever occurs first. This express warranty is extended by Cactus Technologies® Limited to customers of our products.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of Cactus Technologies® responsibilities regarding the Cactus Technologies® OEM Grade Flash Storage Products. Cactus Technologies®, at its sole option, will repair, replace or refund the purchase price of the defective product. Cactus Technologies® guarantees our products meet all specifications detailed in our product manuals. Although Cactus Technologies® products are designed to withstand harsh environments and have the highest specifications in the industry, they are not warranted to never have failure and Cactus Technologies® does not warranty against incidental or consequential damages. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or backup features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective, Cactus Technologies® will have the option of repairing, replacing or refunding the purchase price the defective product, if the following conditions are met:

A. The defective product is returned to Cactus Technologies® for failure analysis as soon as possible after the failure occurs.

B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.

C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding maximum ratings or operating conditions.

All failing products returned to Cactus Technologies® under the provisions of this limited warranty shall be tested to the product’s functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs. Cactus Technologies® Limited may repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

IV. RECEIVING WARRANTY SERVICE

According to Cactus Technologies® warranty procedure, defective product should be returned only with prior authorization from Cactus Technologies® Limited. Please contact Cactus Technologies® Customer Service department (tech@cactus-tech.com) with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, Cactus Technologies® will issue a Return Material Authorization or Product Repair Authorization number and shipping instructions.