Cactus Technologies® White Paper

CTWP016: An Overview of Pseudo-SLC NAND

1 Introduction

When it comes to the choice of flash storage solution for industrial and/or embedded applications, system designers generally have two choices – products using SLC NAND or those using MLC NAND. SLC NAND flash has very high endurance, is very reliable and can work over extended temperature range. However, the cost of SLC NAND products can be prohibitive at high capacities.

For those projects that are cost sensitive, designers sometimes look to MLC NAND products as an alternative. MLC NAND offers high capacity at low cost. The trade off, however, is that MLC NAND has low endurance (less than 1/20 that of SLC NAND), has high error rates and does not work well over extended temperature range.

For some time now, flash storage vendors have promoted a third option, which is some sort of enhanced MLC NAND product. These have been marketed under various names – enhanced MLC, iSLC, superMLC, MLC+, turbo MLC, etc. Recently, pseudo-SLC (a.k.a. pSLC) has been heavily promoted by various vendors. This has been confusing for many users as it is unclear what the underlying technology is and whether all these different products are the same thing.

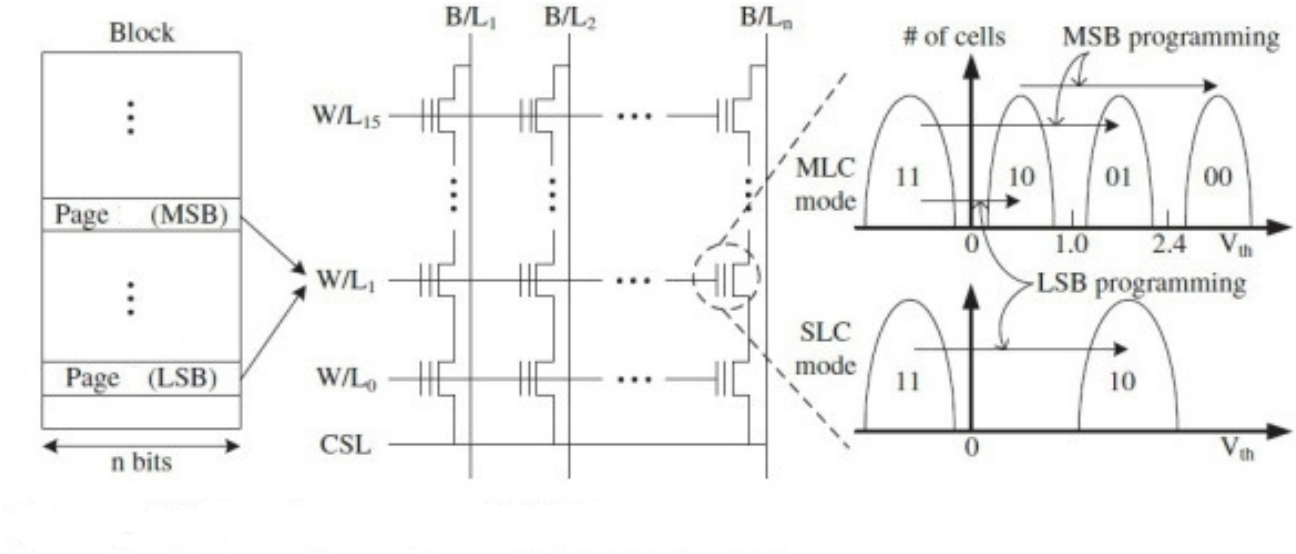
In this whitepaper, we will try to explain the underlying technology for pSLC and how it differs from other 'enhanced' MLC technology.

2 NAND Flash Basics

In order to better understand pSLC technology, we first need to understand how MLC NAND is organized and programmed.

2.1 NAND Flash Structure

NAND flash is internally organized in blocks and pages. Each block contains multiple pages, depending on the device capacity; a typical number is 64 to 256 pages per block. Each page has a fixed size; current MLC NAND has a page size of either 8KB or 16KB, depending on device capacity.

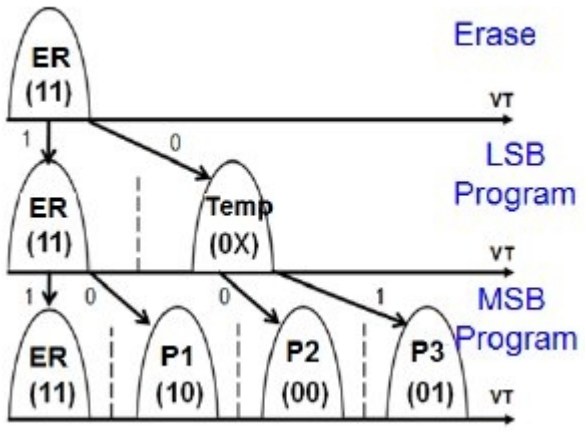


2.2 MLC NAND Programming

Each cell in an MLC NAND can be programmed to store two bits of data; these two bits come from two different pages. The LSB is programmed first, this puts the memory cell in an intermediate programmed state. This programming step is known as low page or fast page programming. This programming step is fairly fast because the intermediate programmed state does not have to be very precise, the threshold voltage just need to be high enough for the sensing circuit to distinguish it from the erased state.

The MSB is programmed next, this is known as high page or slow page programming. This programming step is slow for two reasons. First, a read operation must be performed to find out whether the LSB is '0' or '1'. Second, this programming step has to precisely place the cell in one of three possible states; this requires a programming algorithm that incrementally move the cell threshold in multiple passes.

Fig 2: MLC NAND programming sequence



Taken together, the LSB/MSB programming sequence results in an MLC write throughput that is much slower compared to SLC NAND programming.

3 Fast Page Mode

Now that we have seen how MLC NAND is programmed, it then becomes apparent that it is possible to use an MLC NAND to store only one bit of data by simply not programming the high page. Using an MLC NAND this way is know as 'Fast Page Mode'. In fact, some vendors have been promoting this product under various different marketing names, such as 'turbo mode', MLC+, etc.

The advantage of Fast Page Mode is that this can be done with any MLC NAND flash, it does not require any special commands. It provides a simple way of achieving performance boost by trading off device capacity. The downside is that there is only a slight improvement in device endurance as compared to a true SLC NAND flash. This is because the threshold voltage of the intermediate programmed state is not as high as that of SLC NAND. Also because of this, the error rates and data retention of Fast Page Mode NAND is not much better than that of standard MLC NAND.

4 pSLC Mode

In pSLC mode, the memory cell is also used in single bit mode but with the added twist that the programmed threshold is shifted higher also; this is illustrated in the following diagram:

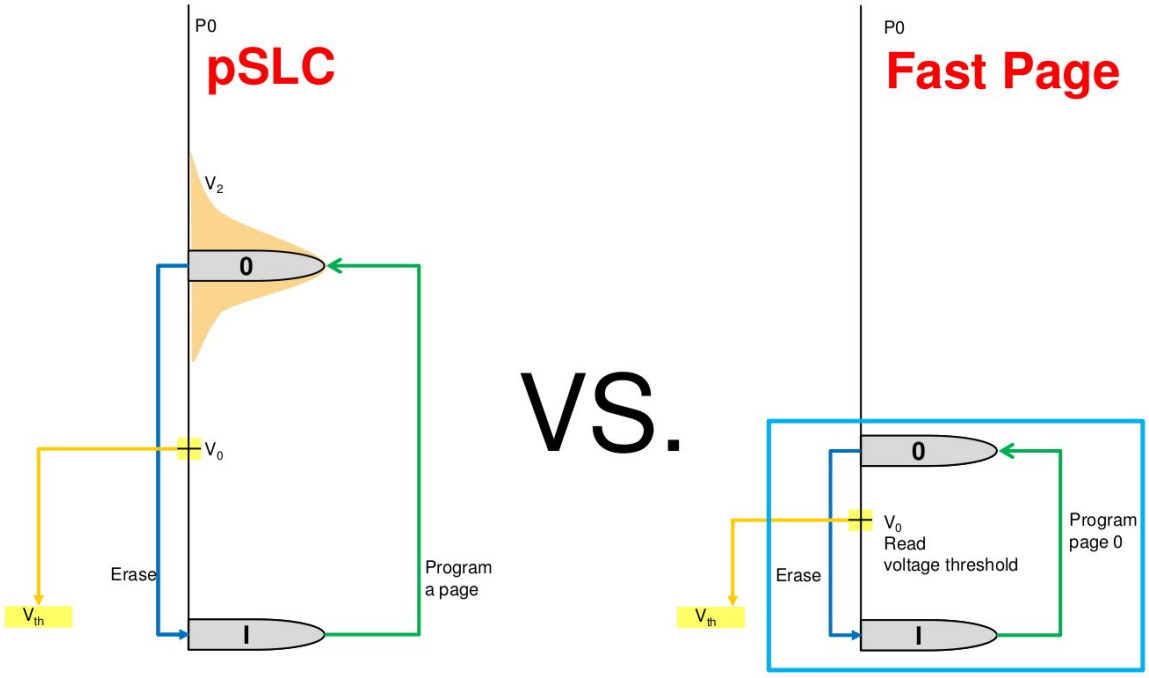


Fig 3: pSLC vs Fast Page

This shifting of the programmed threshold voltage to a higher value has many advantages. It increased the sensing margin between the programmed state vs the erased state, thus resulting in higher endurance, lower error rates and longer data retention. All these are a result of the larger noise margin due to the higher programmed threshold.

The shifting of the sensing threshold and higher programming threshold requires a special vendor command that is specific to each vendor's MLC NAND. Thus, unlike Fast Page Mode, pSLC mode cannot be used on any MLC NAND, it is available only on those MLC NAND where pSLC mode is specifically enabled by the vendor.

5 pSLC Mode vs Fast Page Mode

The following table summarizes the differences between pSLC Mode and Fast Page Mode NAND:

Feature	Fast Page Mode	pSLC Mode
Performance	Better than MLC	Better than Fast Page Mode
Availability	Any MLC NAND	Specific MLC NAND supported by vendor
Endurance	Slightly better than MLC	2X to 7X better than MLC

Feature	Fast Page Mode	pSLC Mode
Error Rates	Slightly better than MLC	Much better than MLC
Data Retention	Slightly better than MLC	Much better than MLC

6 pSLC mode vs 100% Over Provisioning (OP)

As pSLC mode is using MLC NAND in half its intended capacity, the question arises as to whether an MLC NAND that is 100% over provisioned (i.e. the physical capacity is double the user capacity) will achieve the same characteristics as a pSLC NAND. The answer is no.

A 100% OP NAND is still using the NAND in standard MLC mode, thus it does not have the performance gain that pSLC NAND has. Furthermore, as 100% OP NAND is just standard MLC NAND, it has the same high error rates and low data retention issues as standard MLC NAND. As for endurance, the 100% OP NAND will double the endurance as compared to standard MLC NAND but a properly configured pSLC NAND can achieve an endurance that is more than 2X that of standard MLC NAND.

The only scenario where a 100% OP NAND may have better endurance than a pSLC NAND is in situations where the device firmware is using block based mapping and the workload consists of mostly random, small block writes. In such a usage model, the Write Amplification Factor is very high and having double the number of blocks for wear leveling in a 100% OP NAND may help it achieve higher endurance than a pSLC NAND. In all other scenarios, pSLC NAND should have better endurance characteristics.

7 Summary

While most system designers would like to use SLC NAND products for their industrial embedded applications, the high cost associated with such products is driving some some designers to look for cheaper alternatives. MLC NAND products have not been able to meet the reliability and endurance requirements of these industrial applications.

Recently, flash memory vendors have increased their support for pSLC mode in their MLC NAND products. In this whitepaper, we have explained the technology behind pSLC NAND and showed that its characteristics are somewhere between SLC NAND and standard MLC NAND. This may be a viable option for system designers who need a solution that is lower cost than SLC but has more reliability than MLC.

8 Version History

Version	*Date*	*Change*

Version	*Date*	*Change*
1.0	Nov. 1, 2016	Initial Version